Bias Boosting Technique for a 1.9GHz Class AB RF Amplifier

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Abstract

A bias boosting technique for a 3.2V, 1.9GHz Class AB RF amplifier designed in a 30GHz BiCMOS process is presented in this paper. In a Class AB amplifier, the average current drawn from the supply depends on the input signal level. As the output power increases so does the average currents in both the emitter and the base of the power transistor. The increased average current causes an increased voltage drop in the biasing circuitry and the ballast resistor. This reduces the conduction angle in the amplifier, pushing it deep into Class B and even Class C operation, reducing the maximum output power by 25%. To avoid the power reduction, the amplifier should have a larger bias which inevitably has a larger power dissipation at low output power levels. The proposed bias boosting circuitry dynamically increases the bias of the power transistor as the output power increases. The amplifier has less power dissipation at low power levels with an increased maximum output power.

1. Introduction

In an ideal Class B amplifier, the transistor operates as a current source with a conduction angle of 180^o and an amplitude proportional to the input signal [1]. At the presence of a tuned circuit at the output, a Class B amplifier has a linear input-output relationship and provides a high efficiency, theoretically equal to 78.5%. To avoid crossover distortion, the transistor is not biased at the edge of conduction. It is usually biased at a small quiescent current with a conduction angle slightly greater than 180^o. Under these conditions, the transistor is referred to operate in Class AB mode. Class AB amplifiers have been widely used in RF applications [2-5].

RF power transistors are usually interdigitated to reduce the base (or gate) resistance. In bipolar transistors the use of many small emitters can create hot-spotting and lead to a thermal runaway [6]. To prevent this, ballasting resistor is often used i.e. a resistor is introduced in series with each emitter (or base) to divide the current evenly among the emitters [1,7].

ISLPED 2000, Rapallo, Italy.

2. Conventional Class AB

Fig. 1 shows the schematic of an amplifier with a current mirror bias: Q0 is the amplifying transistor, R0 the ballast resistor, L0 the ground inductance, R5 the base biasing resistor, and R2 the load resistor. Due to the exponential nature of the I-V characteristic of BJTs, current mirror biasing is used to bias Q0 in Class AB mode. R4 and R6 are N times larger than R5 and R0 respectively, and Q1 is N times smaller than Q0. The bias current of Q0 is, therefore, N times the current of Q1.

As the input RF signal V2 is increased, the output voltage V0 increases. Fig. 2a shows the power gain, and also rms and average collector currents in Q0 versus output power for a supply voltage of 3.2V and an input frequency of 1.9GHz. The dc current increases as the output power increases resulting in a dc voltage increase in the bias resistance of R5 (15 ohm) and emitter ballast R0 (50 mohm) (Fig. 2b). In large signal operation, we can say that as the RF signal V2 is in its positive half-cycle, Q0 is conducting and it loads the input signal source. For the negative half-cycle of V2, Q0 is off. The input matching network has a series capacitor to isolate the dc path of the amplifier from the input signal. During the positive half-cycle of V2, this capacitor is charged through Q0. During the negative half-cycle of V2 (when Q0 is off), this capacitor is discharged through R5. As R5 is larger than the impedance of Q0 in the positive half-cycle (in our design 15 ohm compared to 5 ohm), the negative swing at base of Q0 is larger than its positive swing. This provides a positive DC current through R5 which has an average value equal to the dc current of the base of Q0. In other words, the dc voltage drop at base of Q0 is necessary to draw the dc current

from the bias circuitry. However, this bias drop reduces the conduction angle of transistor Q0, pushing the transistor deep into Class B and even Class C. This makes it more difficult for the input RF signal to increase the output power.

3. Bias Boosting Technique

In this paper, we present a bias boosting technique to provide extra dc current required in Class AB as the output power is being increased. Fig. 3 shows the same Class AB as in Fig. 1 with the added ideal bias boost circuitry consisting of a voltage-controlled current source G0, and a dc voltage source V1 with a value equal to the amplitude of the RF signal V2. Under this ideal bias boosting condition, as the amplitude of the RF input is increased, so does the dc current generated by G0 which provides for the extra dc current in Q0.

By comparing Figs. 4a-4b with Figs. 2a-2b, we can see that the bias boosting technique increases the maximum output power (2.5W compared to 2W). It should be pointed out the same maximum output power could have been achieved without bias boosting, if the bias circuitry had been designed to provide higher dc current: 600mA compared to 170mA (please refer to Figs. 5a-5b). This extra dc current at low output powers is undesirable. It pushes the transistor deep into Class A and causes excessive power dissipation. Considering the 3.2V supply voltage, the extra 430mA dc current translates into 1.3W of power dissipation.

4. Class AB amplifier with bias boosting

The practical realization of the bias boosting circuitry for a 1.9GHz Class AB amplifier in a 30GHz BiCMOS process is described in this section. Fig. 6 shows a two stage amplifier consisting of a driver transistor Q5 and a power transistor Q0. Q5 is also biased in Class AB. Transistor Q6 is in parallel with Q5 and is M times smaller. Q6 senses the current of the driver. As the input drive signal increases so does the current in Q6. This current is then averaged, scaled and mirrored to be added to the current bias of the power transistor (shown as the Ave./Mirror block in Fig. 6). The function of averaging, scaling and mirroring is done by the use of resistors and capacitors (RC time constants), PNP and NPN transistors in current mirror configurations. The power dissipation in the Ave./ Mirror block is small (less than 80 mW at maximum power) because of the scaling factor N used in the bias circuitry of the power transistor.

Figs. 7a,7b & 7c show the rms and average collector currents in Q0, average voltages, power added efficiency (PAE) and power gain, when bias boosting is off and using an ideal off-chip matching network. Figs. 8a, 8b & 8c show the results when bias boosting is applied. Bias boosting increases the maximum output power from 1.6W to 2.2W. It also increases the PAE at maximum output power from 57.5% to 61.5%. The same 2.2W maximum output power could have been achieved without bias boosting, if a larger current (700mA compared to 170mA) had been provided to the power transistor. However, this extra current causes excessive power dissipation at low output power levels.

5. Conclusion

In a bipolar Class AB amplifier, the dc current increases as the output power increases resulting in a dc voltage drop in the bias circuitry and ballast resistance. Therefore, the conduction angle reduces as the output power increases. As the transistor is pushed into Class C operation, the maximum output power is reduced. The higher the resistances on the dc path of the currents of base and emitter are, the higher the power reduction is. To have Class AB operation at high output power requires the transistor to have a large bias. This results in an unnecessary higher power dissipation at low output powers. It is shown that a bias boosting technique can be used to compensate the excess voltage drop in the bias circuitry as the output power increases. Current sensing of the driver stage is used to extract the signal level applied to the power stage. This current is averaged, scaled and then used to increase the bias voltage of the power transistor. Simulations indicate that for a 3.2V, 2W, 1.9GHz Class AB amplifier the maximum output power is increased by 25%.

References

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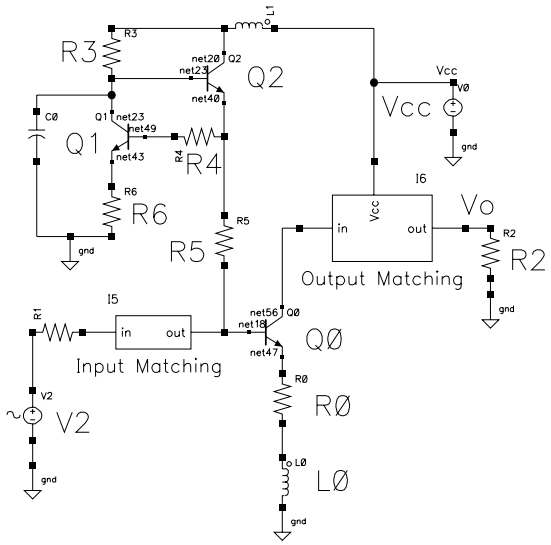

Fig. 1: Conventional Class AB amplifier

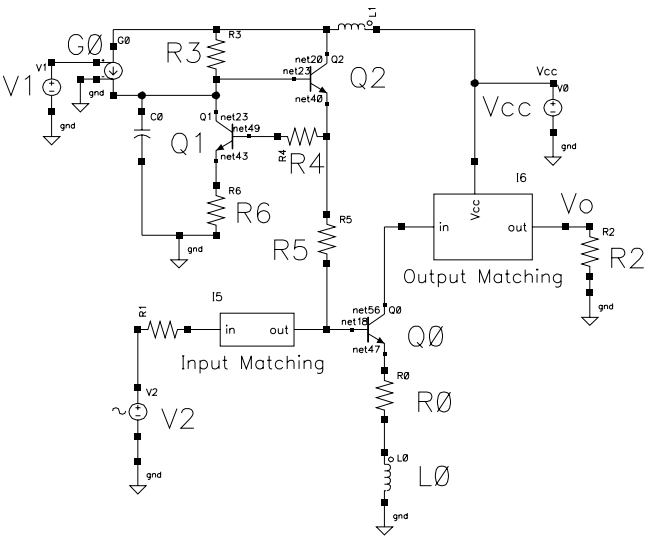

Fig. 3: Ideal Bias Boosting in Class AB amplifier

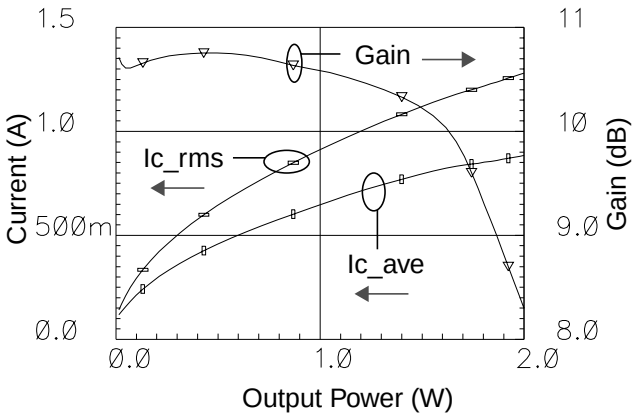

Fig. 2a: Currents and Gain in conventional Class AB

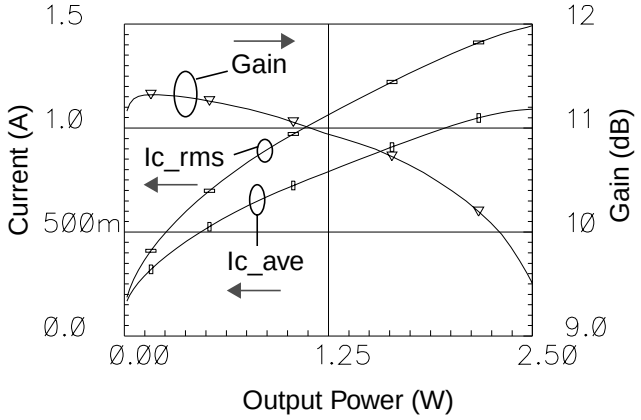

Fig. 4a: Currents and Gain in bias boosting Class AB

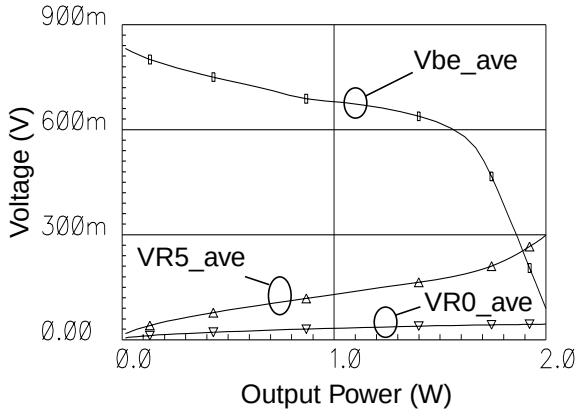

Fig. 2b: Average voltages in conventional Class AB

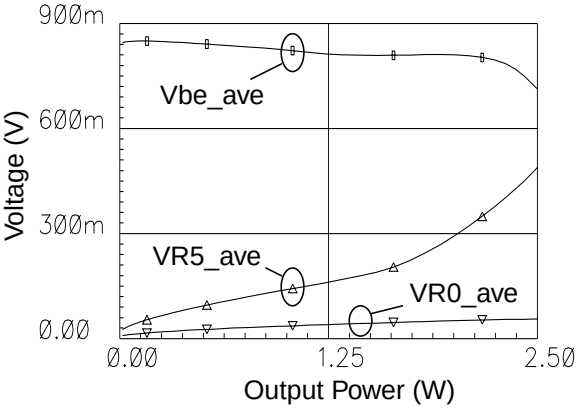

Fig. 4b: Average voltages in bias boosting Class AB

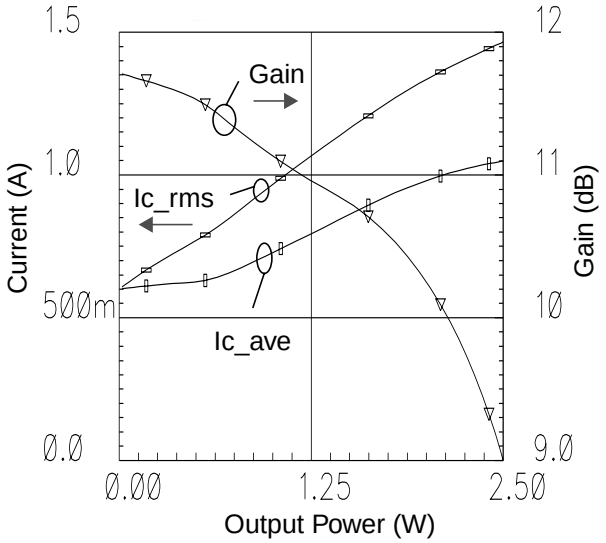

Fig. 5a: Currents and Gain in Class A amplifier

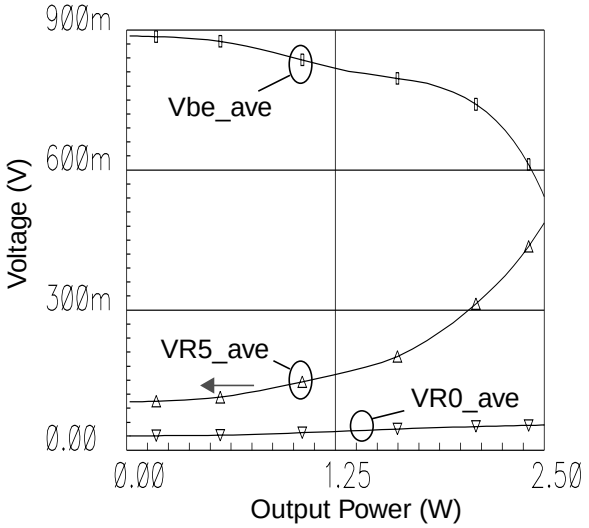

Fig. 5b: Average voltages in Class A amplifier

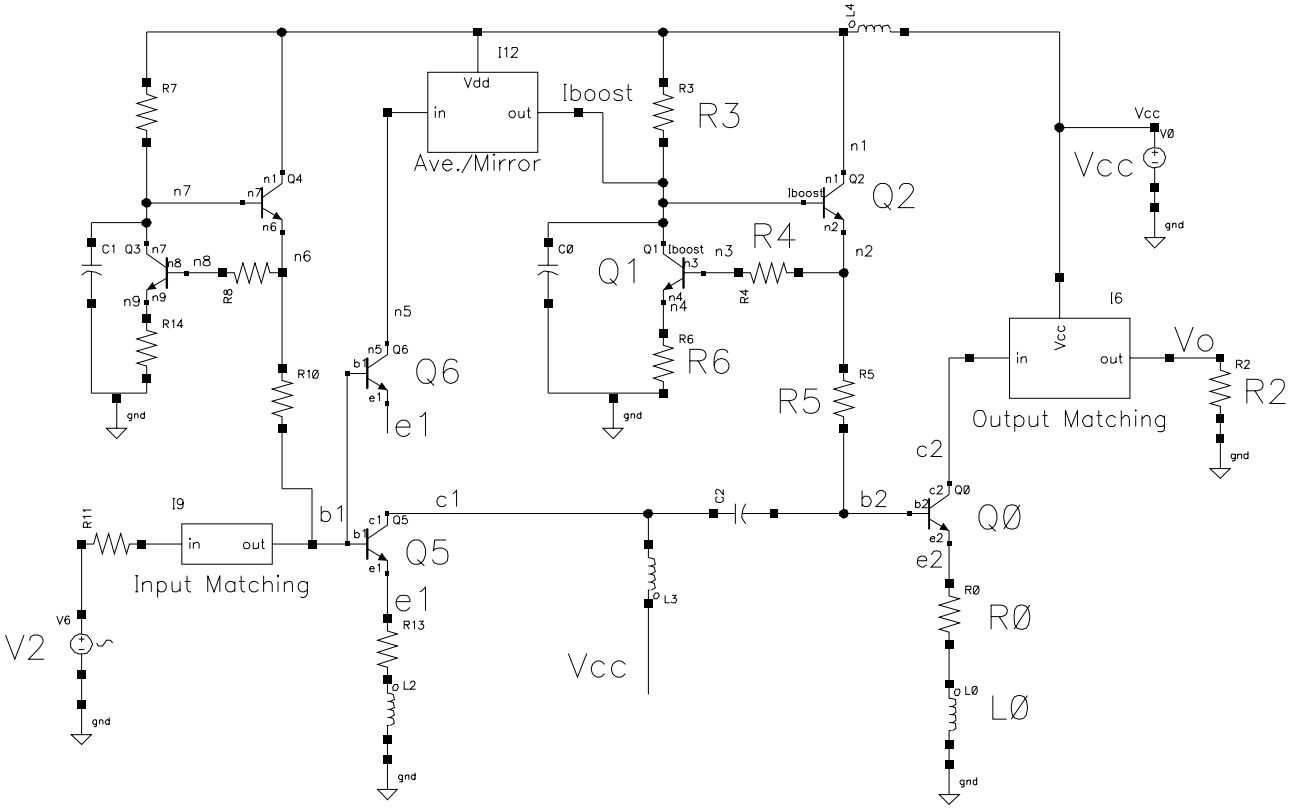

Fig. 6: Two stage Class AB amplifier with bias boosting

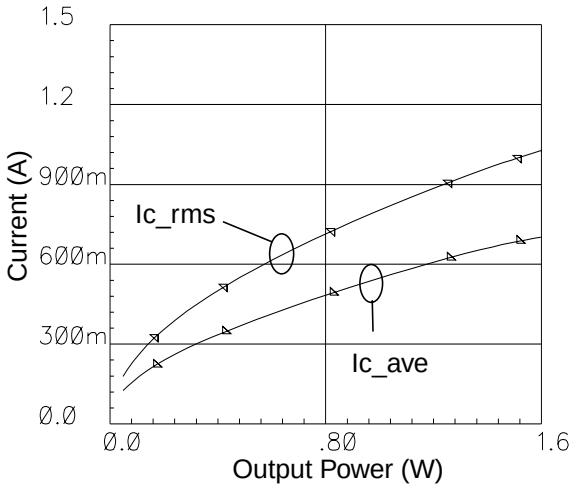

Fig. 7a: Currents in two-stage conventional Class AB

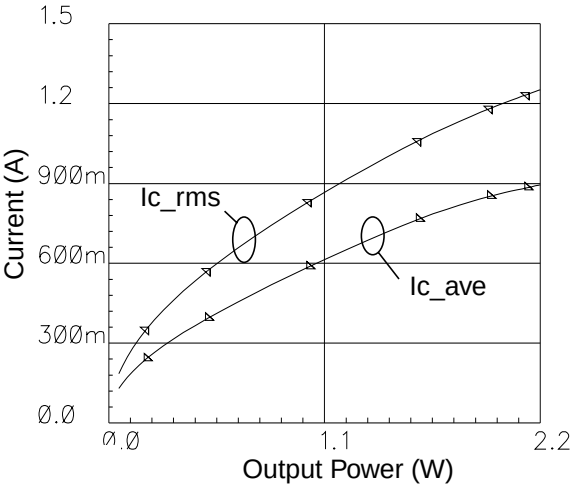

Fig. 8a: Currents in two-stage bias boosting Class AB

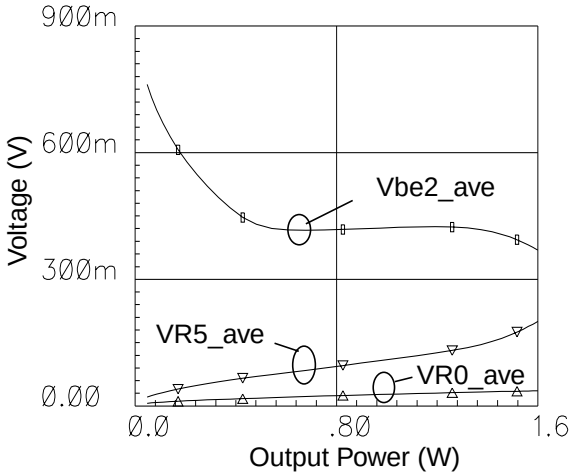

Fig. 7b: Voltages in two-stage conventional Class AB

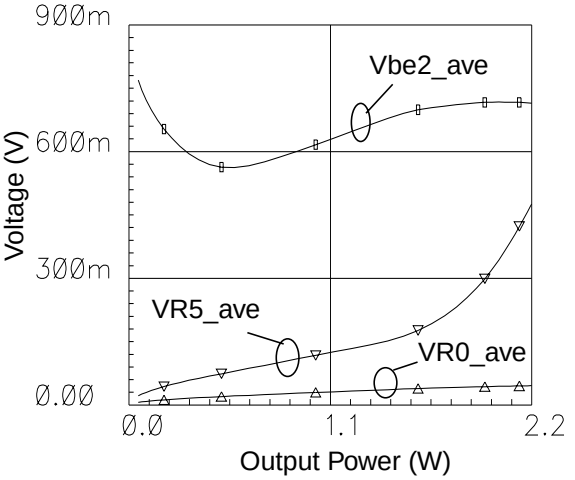

Fig. 8b: Voltages in two-stage bias boosting Class AB

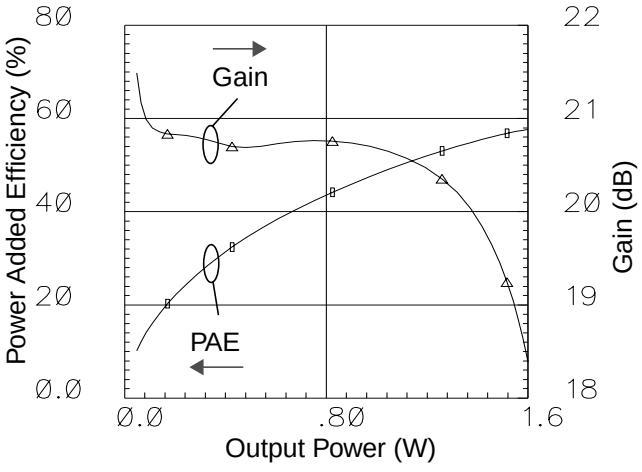

Fig. 7c: Power Added Efficiency and Gain in two-stage conventional Class AB

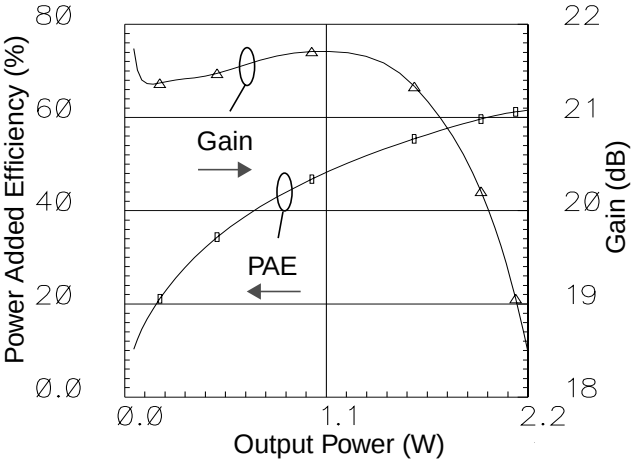

Fig. 8c: Power Added Efficiency and Gain in two-stage bias boosting Class AB