ASP-DAC 2000 Best Paper Award Candidates

E7.1 "A 12b 50 MHz 3.3V CMOS Acquisition Time Minimized A/D Converter", Young-Deuk Jeon, Byeong-Lyeol Jeon, Hyoung-Kyu Choi, Seung-Hoon Lee (Sogang Univ., Korea) [LSI Development]

A6.1 "Optimization of VDD and VTH for Low-Power and High Speed Applications",
Koichi Nose, Takayasu Sakurai (Univ. of Tokyo, Japan) [Designs]

B2.1 "A New Method for Constructing IP Level Power Model Based on Power Sensitivity",
Heng-Liang Huang, Jiing-Yuan Lin, Wen-Zen Shen, Jing-Yang Jou (Nat'l Chaio-Tung Univ., Taiwan) [Design Methods & Environments]

C5.1 "Performance-Optimal Clustering with Retiming for Sequential Circuits",
Tzu-Chieh Tien, Youn-Long Lin (Tsing Hua Univ., Taiwan) [Logic Synthesis]

D3.1 "Delay-Optimal Wiring Plan for the Microprocessor of High Performance Computing Machine",
Jun Kikuchi, Tetsuo Sasaki, Tohru Hashimoto, Kazuhisa Miyamoto (Hitachi, Japan) [Physical DA]

D6.1 "A Cell Synthesis Method for Salicide Process",
Kazuhisa Okada, Takayuki Yamanouchi, Taksahi Kambe (Sharp, Japan) [Physical DA]

E4.2 "Circuit Performance Oriented Device Optimization using BSIM3 Pre-Silicon Model Parameters",
Mikako Miyama, Shiro Kamohara, (Hitachi, Japan) [T-CAD]