Substrate Crosstalk Analysis in Mixed Signal CMOS Integrated Circuits

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Abstract — Substrate crosstalk modeling and analysis techniques for a reliable SoC oriented mixed signal IC design are outlined. Substrate noise measurements by use of a source follower and a latched comparator clearly indicate that $L \cdot di/dt$ and $R \cdot i$ effects on Vdd/Gnd wirings appear in the substrate. An experimental full chip substrate crosstalk verification system based on a macroscopic substrate noise model efficiently analyzes the analog performance degradation relevant to the digital activity on the same chip.

I. Introduction

Successful systems-on-a-chip (SoC) VLSI designs necessitate reliable substrate crosstalk handling. Issues raised by the crosstalk extend to both of the analog and digital regions, where analog performance degradation, dynamic logic failure, detriment to signal integrity, and so on, are included. As the technological advance in CMOS manufacturing allows practical integration of analog functional cores along with million gate digital macros in IP based reusable designs, those have been becoming recognized widely as serious problems to be solved with a higher priority.

Developments of full chip substrate crosstalk verification techniques must be a key to provide general solutions. Here, efficient estimations of the system performance with the crosstalk influence is valid especially in early design stages for optimizing floorplans, timing designs, and operation margins. Time-domain analyses will be helpful for investigating irregular incorrect operations that may correlate to certain digital functions or output patterns, for instance. However, the crosstalk analysis needs to analyze the whole system including all active circuits within a chip and distributed passive elements parasitic to the substrate and also to the surroundings. Therefore, compact simulation models are necessary.

Principal constituents of the substrate crosstalk model comprise substrate noise injection, substrate coupling, and substrate sensitivity. Dominant noise sources are digital blocks and output buffers that inject noise currents into the silicon substrate. The currents spread in the substrate and drain off to the system ground via distributed substrate contacts at the surface and metallic wires. Consequently, voltage variations around the injected points propagate in the substrate and also potential gradients arise due to a resistive nature of the substrate. The time variant substrate voltages are sensed by MOSFETs through body effects and transferred to signal paths in consequence of current fluctuations or gain mismatches in analog circuits, thus appear as the substrate crosstalk. On the other hand, sub-threshold current increase due to the body bias change may cause dynamic operation failures and thus degrade digital signal integrity seriously.

The aforementioned processes have been clearly observed by Su et al. [1], where simple noise injection to the substrate via capacitive coupling and noise detection by a MOSFET current source are used in their experimental structure. As for the noise propagation in silicon substrates, quantitative evaluation of guardband effects in a lightly doped substrate and also in a heavily doped substrate with a lightly doped epitaxial layer on top has been performed. Results were well fit to device simulations where Poisson equation is numerically solved for the substrate [1], and also fit to circuit simulations with a substrate equivalent resistive mesh [2]. A simpler resistive coupling model has been proposed in [3], which can reproduce measurement results with a similar experimental structure in frequency domain analyses up to a few GHz. It is proved by these reports that the substrate itself can be treated as a resistive material as long as circuits work in a base-band frequency range.

Modeling of the noise injection is controversial. Models simple enough to cover thousands of logic gates have been developed among existing substrate noise simulation systems targeting a full chip analysis, as summarized bellow. Major probable noise current sources are (1) Capacitively Coupled (CC) currents through parasitic capacitances against the substrate consisting of MOSFETs' S/D diffusions and lower level metal wirings, (2) Impact Ionized (II) currents at the drain ends of MOSFETs, and (3) voltage bounce on supply/return rails coupled to the substrate via the well to substrate capacitance and via substrate contacts, respectively [4], [5]. The former two occur at every gate switching independently and it is shown in [6] that CC currents becomes more dominant than II currents when switching frequency is larger than 10MHz for an inverter in a quarter micron CMOS technology. Models emphasizing CC like "SubWave" [7] represent the noise

injection in digital blocks as a linear superposition of microscopic contributions to the substrate noise per a gate switching.

On the contrary, interaction between currents and parasitic impedances on the supply/return wirings determines the noise injection in (3). A model that deals with the parasitics of entire power supply distribution and logic gates as current switches has been proposed in "RAIL" [8], where an overall system response is computed in Laplace domain with a moment matching technique [9], [10]. Rapid substrate noise estimation by use of average supply currents extracted from pre-computed power dissipation analyses reported in [11] is a straight realization of this class.

The other approach applies a behavioral expression to the substrate noise, which has a great possibility in improving the efficiency. Transition frequency for the target digital block is obtained from the event driven logic simulator, and is used for the substrate noise synthesis [12], [13].

For choosing the best way to model the noise injection, experimental understanding of the substrate noise properties must be necessary.

Susceptibility of the circuits to the substrate crosstalk can be evaluated by transistor level simulations, where the computed substrate voltage is applied to the back gates of MOSFETs. Use of the behavioral modeling for the circuit response to the substrate voltage can improve computing efficiency for those substrate crosstalk analyses, where the voltage is included as one of the state variables [14].

The rest of the paper focuses on the current understanding of the substrate crosstalk based on high resolution measurements and our experimental HDL-based simulation system for the full chip verification.

II. Substrate Crosstalk Measurements and Analyses

A. Noise Source and Detector Circuits

A transition controllable noise source shown in Fig. 1 was developed [15]. The circuit has a multi-phase clock (Ck[0:10]) generator consisting of odd delay elements in series, and a matrix of noise source blocks. The delay element has bias voltages V_n and V_p for regulating rise and fall delay, respectively. Inverting and non-inverting outputs are selectable among Ck[0:10]. The address signal x[0:3] sets the number of active blocks in the noise source matrix.

The noise source block includes 30 inverters in parallel where the inverter has a 50fF load capacitor against the substrate corresponding to 2 gate input capacitances with $400\mu m$ AL1 wires. Multiple drivers are provided between the delay elements to the inverters, in order to guarantee 200ps switching time with driving the load capacitor and minimize the delay time dependence.

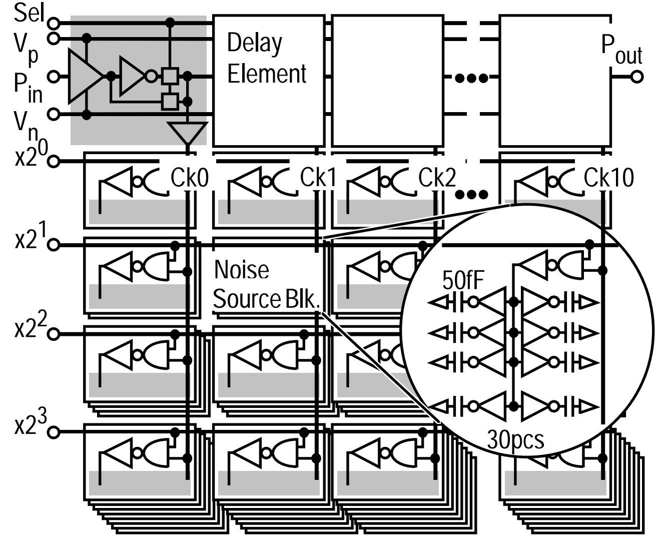

Fig. 1. Transition controllable noise source.

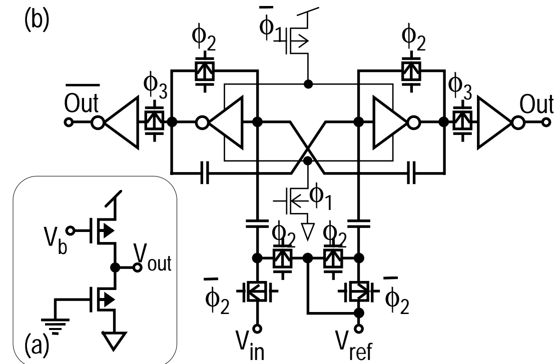

Fig. 2. Substrate noise detectors, (a) a source follower, (b) a latched comparator.

A PMOS source follower (SF) and a differential latched comparator (LC) are used as the substrate noise detector (Fig. 2). SF enables a direct substrate voltage measurement, however, bandwidth limitation is unavoidable because of a gate capacitance at the input and load capacitances added by measurement instruments. A comparator senses a change in the substrate voltage as a shift in the threshold voltage, ΔV_{th} [16], [17]. A large gain of LC resulting from the positive feedback allows a high speed operation. Acquisition of the substrate noise waveform as $\Delta V_{th}(t)$ with a time resolution of $\Delta t = 100$ps was realized.

A micro photograph of a substrate noise evaluation test chip fabricated in $0.4\mu m$CMOS, DPTM, P-substrate N-well technology is shown in Fig. 3.

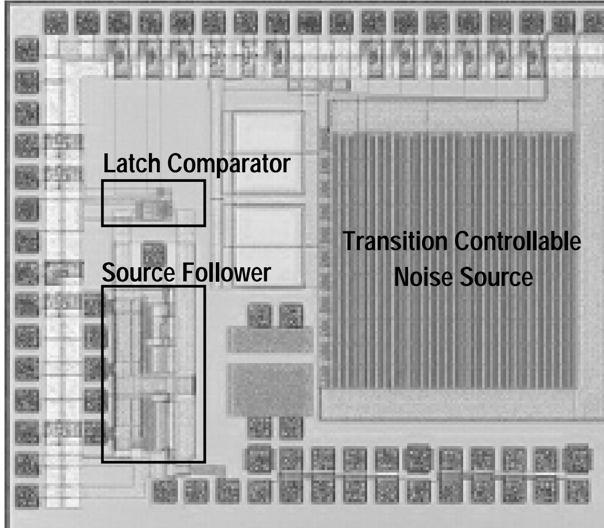

Fig. 3. Substrate noise evaluation test chip.

B. Measurement Results

Figure 4(a) shows a waveform obtained by SF. The multi-phase clock generation is completed between P_{in} given to and P_{out} output from TCNS. Large ringings appear after both of the rise and fall P_{in} edges in the waveform, however, changes corresponding to the transitions inside TCNS are not resolved. On the other hand, 100ps-100μV resolution measurements performed by LC clearly resolve 11 sub-peaks with an around 2.5ns interval as shown in Fig. 4(b). Each sub-peak is a substrate voltage variation from the noise source block activated by the corresponding phase in Ck[0:10].

Fig. 5 summarizes the sub-peak interval T_s, the inter-stage delay T_d calculated from T_{out}, and the peak width T_w at ΔV_{th}=0V for non-inverting (rise only) and inverting operations with the smallest fall to rise delay. Obvious agreement between T_s and T_d proves the on-to-one correspondence in the sub-peaks to the noise source action. The graph shows that T_w is a few times larger than the switching time T_{sw} of 200ps, although all the inverter state transitions involved in the each sub-peak complete at a time. T_w is larger for the inverting operation, because a pair of successive fall and rise state transitions is included in each of the sub-peaks. $T_w < T_s/2$ in a larger delay region indicates that each substrate voltage change arising from the noise source block becomes independent.

C. Substrate Noise Analyses – Ringing

Figure 6(a) shows a simplified circuit schematic of the measurement setup. R, L are lumped parasitics to wires connecting the packaged chip to the power supply. L_{pkg} is inductance parasitic to the assembled chip. C_d is a decoupling capacitor placed adjacently to the chip socket. The most dominant ringing frequencies extracted from waveforms measured by SF for with and without C_d can be roughly fit to $\omega_0 = 1/\sqrt{L_{pkg}C_{par}}$ and $\omega_1 = 1/\sqrt{(L+L_{pkg})C_{par}}$. Here, C_{par} is a total parasitic capacitance between Vdd/Gnd in the noise source circuit. Estimated values are L_{pkg} = 118nH and C_{par} = 320pF.

SPICE simulation results for the circuit with a full transistor description of TCNS shown in Fig 6(b) well repro-

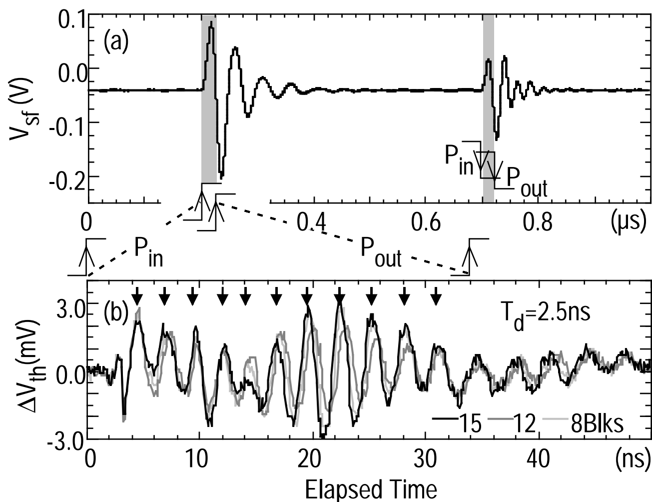

Fig. 4. Substrate noise waveforms, (a) obtained by SF, and (b) by LC.

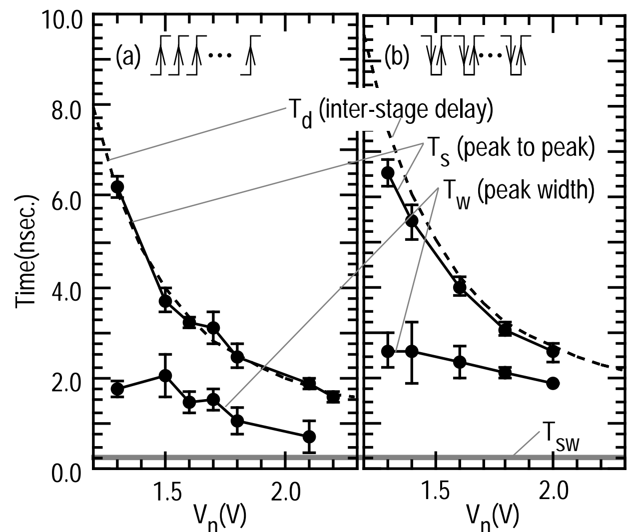

Fig. 5. Measurement results for (a) rise operations, and (b) inverting operations.

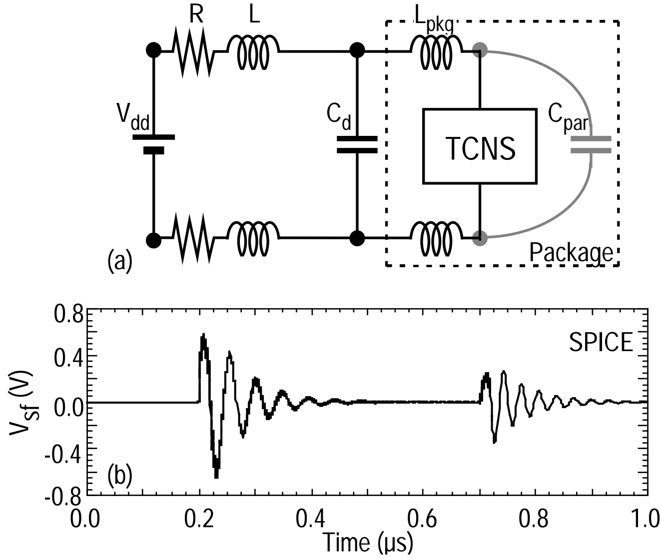

Fig. 6. Ringing analysis, (a) a simplified circuit, and (b) a SPICE simulation result.

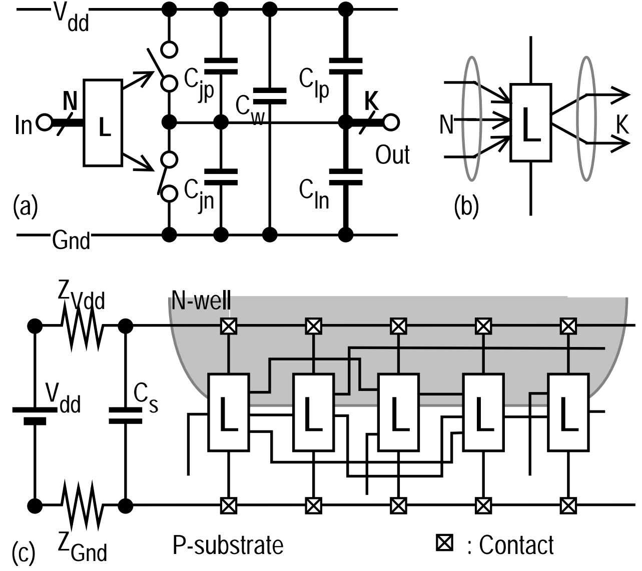

Fig. 7. Equivalent circuits, (a) a logic element and its (b) symbol, (c) a logic block.

duce the measured waveforms given in Fig. 4(a). Note that the difference in the ringing frequencies at the rise and fall edges comes from the difference in C_{par} for the rise and fall transitions due to the 50fF load capacitance in the noise source element.

It is apparent that the ringing purely arises from $L \cdot di/dt$ effect on the Vdd/Gnd paths and appears in the substrate through substrate contacts. Optimized decoupling circuits can well dump those ringings [18] – [20], and the simplified circuit model used here is helpful for the optimization.

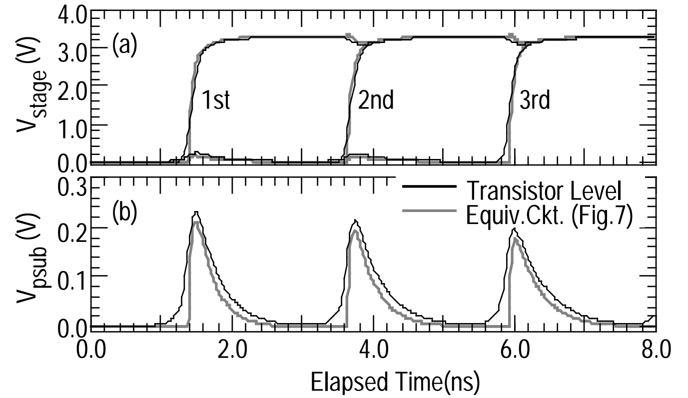

Fig. 8. SPICE Simulation results, (a) output voltage in the first three stages, (b) substrate voltage.

D. Substrate Noise Analyses – Sub-peaks

Fig. 7 shows equivalent circuits of logic elements and a digital block. Switching to charge or discharge the load capacitance determines logical output. Here, **L** selects a logical state from a truth table for **N** inputs.

In CMOS logic, the switches are realized by N/PMOS (with channel resistance), and the load capacitance consists mainly of drain capacitance C_{jn}, C_{jp}, well capacitance C_w, and the sum of input and wire capacitance of following **K** logic elements C_{ln}, C_{lp}. C_s is parasitic to packages and wires by an assembly. Z_{Vdd}, Z_{Gnd} are lumped impedance parasitic to the supply(Vdd) and return(Gnd) paths, respectively.

When $M_{\uparrow}(T)$ and $M_{\downarrow}(T)$ gates switch in rise and fall during a unit time $T \sim T+\tau$, respectively, charge transfer of $Q(T) = (C_{\uparrow}(T)+C_{\downarrow}(T)) \cdot Vdd$ occurs. $C_{\uparrow}$ and $C_{\downarrow}$ follow bellow.

$$C_{\uparrow}(T) = \sum_{l}^{M_{\uparrow}(T)} (C_{jn,l} + C_{jp,l} + C_{ln,l} + C_{lp,l}) \quad (1)$$

$$C_{\downarrow}(T) = \sum_{m}^{M_{\downarrow}(T)} (C_{jn,m} + C_{jp,m} + C_{ln,m} + C_{lp,m}) \quad (2)$$

Rapid charge redistribution takes place among $C_{\uparrow}, C_{\downarrow}$, and C_{par} in the first place, and then the external supply feeds $Q(T)$ with a time constant τ given roughly by a product of $Z_{Vdd} + Z_{Gnd}$ and C_{par}. Logic state transitions complete around T_{sw} by the former process, while the

latter generates the broad peak in the substrate voltage, as shown in Figs. 4, 5. These processes contribute to reduce the maximum value of the supply current and thus to suppress the substrate voltage variation.

Fig. 8 gives SPICE simulation results. Here, both Z_{Vdd} and Z_{Gnd} are 1Ω without inductance. Consistency between analyses with a full transistor description of TCNS and those with an equivalent circuit description proves that the sub-peaks in the substrate noise arise from $R \cdot i$ effect on Vdd/Gnd paths with the RC relaxation process.

III. Full Chip Substrate Crosstalk Verification

A. Macroscopic Substrate Noise Model

We have proposed a macroscopic substrate noise model shown in Fig. 9. The substrate noise is computed according to a noise waveform function $F(f_{eff}, t)$ and injected to sensitive circuits, in parallel with a transient analysis of the mixed signal circuit under design. $f_{eff}(n)$ defined in Eq. 3 is the effective transition frequency at the n-th sampling interval, where the unit time T is taken as the noise sampling period for descretizing the noise generation process. $N_i(n)$ is a state transition count in the ith digital subblock, and ω is a weight coefficient for the transition direction. Superscripts of +, - stand for rising and falling transitions, respectively.

$$f^i_{eff}(n) = \frac{1}{T}\left[\omega^+ N_i^+(n) + \omega^- N_i^-(n)\right] \qquad (3)$$

An experimental substrate crosstalk verification system based on the macroscopic substrate noise model has been implemented on a commercial mixed signal simulation environment, as shown in Fig 10. Description languages are Verilog-HDL for digital parts and a hybrid of Verilog-A/SPICE for analog parts. Bold lines are analog/digital signal paths, while narrow lines and shaded boxes stand for the substrate noise computation paths and modules, respectively.

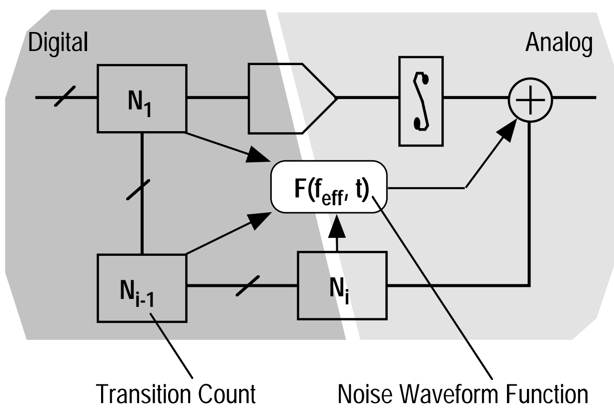

Fig. 9. Macroscopic substrate noise model.

A transition count routine (TC) is assigned to each of the digital subblocks. It monitors state transitions in the digital subblock and returns f_{eff} to a substrate noise generator (NoiseGen) in every T. The substrate noise $F(t)$ injected to the analog parts is expressed as a linear superposition of contributions $\Phi(t)$ from every digital subblock multiplied by relative substrate coupling intensity coefficients W between the subblocks to the sensitive circuit (Eq. 4).

$$F(t) = \sum_{i=1}^{m} W_i \Phi_i\left(f^i_{eff}, t\right) \qquad (4)$$

The supply/return bounce described in the previous section has to be expressed in $\Phi(t)$, where the averaged supply currents approximated from f_{eff} and interaction with the lumped LCR should be included. The coefficient W represents noise amplitude attenuation by the distances and guardbanding. It can be estimated by circuit simulations with efficient substrate macro-models or otherwise by point-to-point substrate impedance extraction methods [21] – [26].

B. Verification Example

ADC conversion performance degradation is simulated with the macroscopic substrate noise model. Figure 11 shows a testbench where the 2nd order $\Delta\Sigma$ADC with 4MHz oversampling frequency (F_{os}) is coupled to a digital noise source having 545 inverters.

Two verification approaches are tested: *Type-I* uses an ADC model in a full analog-HDL description where the

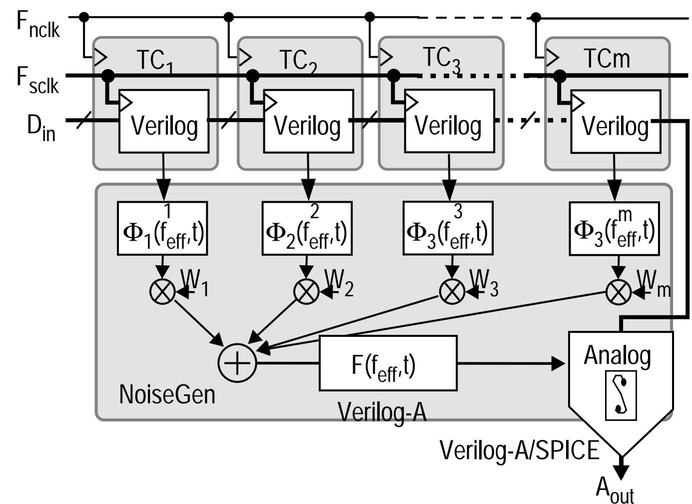

Fig. 10. Simulation system block diagram based on the macroscopic substrate noise model.

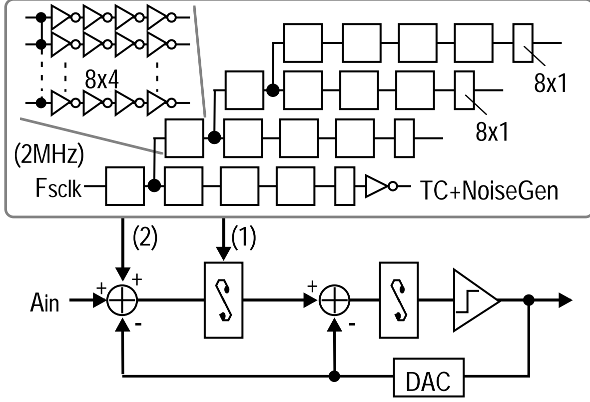

Fig. 11. Simulation testbench: the 2nd order ΔΣADC coupled to the digital noise source.

computed noise is added to state variables, and *Type-II* uses a transistor level description selectively to the susceptible parts such as the amplifier in the first integrator. *Type-I* is appropriate for verifications necessitating the long period transient analyses. Examples include quantifying Signal to Noise Ratio (SNR) or Bit Error Rate (BER), estimating the noise intensity from the digital processing amount, and timing optimization between analog and digital clocks. On the other hand, *Type-II* is able to simulate a precise response to the noise and is appropriate for such as a sensitivity evaluation based on repetitious short period transient analyses.

Figure 12 shows FFT spectrums simulated in *Type-II*, where the noise source is inactive in (a), is activated during 10 cycles of 2MHz clock in every 100μs in (b), and is activated during 10 and 15 cycles of 2MHz clock alternatively in every 100μs in (c). The noise source activation frequency of 10kHz and its harmonics are found in (b), and the modulation frequency of 5kHz and its harmonics also appear in (c). Although the noise source operates with a clock frequency far outside the ADC's bandwidth, periodic appearances of large scale processing with frequency inside the bandwidth produce those frequency components in the signal spectrum through the substrate coupling.

ADC performance is very sensitive to the phase difference between the system and the oversampling clocks [27]. SNR dependence on the phase difference simulated with *Type-I* indicates the significance of the timing optimization in the mixed signal IC designs (Fig. 13).

An FFT of 1024pts requires a 17ms transient simulation result that costs CPU time of 7 and 10 hours in *Type-I* and *Type-II*, respectively, with UltraSPARC-140MHz. These results clearly prove the effectiveness of HDL-based full chip substrate crosstalk verification.

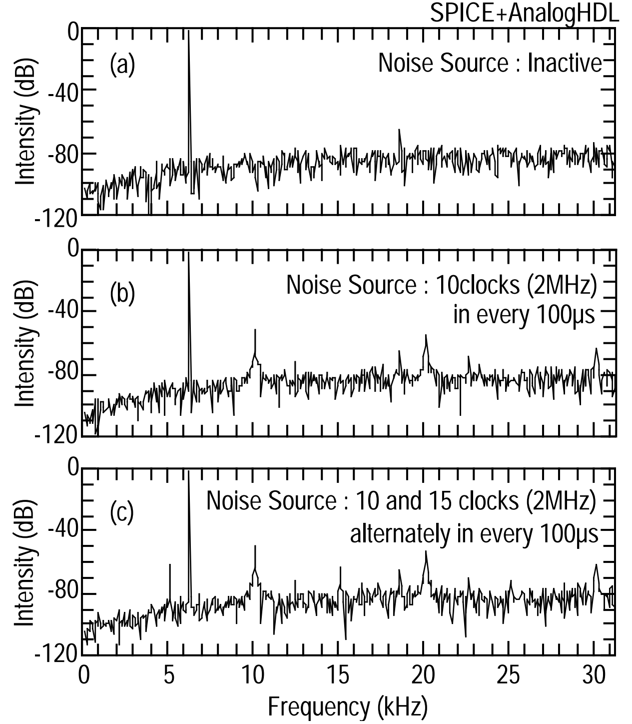

Fig. 12. FFT spectrums.

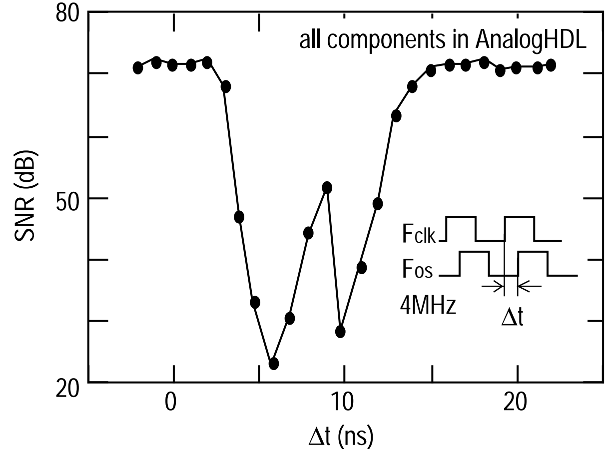

Fig. 13. SNR versus phase difference.

IV. Conclusion

Substrate crosstalk modeling and analysis techniques are outlined.

Substrate noise measurements performed by a source follower and by a latched comparator with 100ps-100μV

resolution clearly indicate that $L \cdot di/dt$ and $R \cdot i$ effects on Vdd/Gnd wirings dominate the substrate crosstalk. Simple circuit models can reproduce these results.

An experimental full chip substrate crosstalk verification system based on a macroscopic substrate noise model efficiently analyzes the analog performance degradation relevant to the digital activity on the same chip.

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References

[1] D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE J. Solid-State Circuits*, Vol. 28, No. 4, pp. 420-430, Apr. 1993.

[2] N. K. Verghese, T. J. Schmerbeck, and D. J. Allstot, "Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits," Kluwer Academic Publishers, 1995.

[3] K. Joardar, "A Simple Approach to Modeling Cross-Talk in Integrated Circuits," *IEEE J. Solid-State Circuits*, Vol. 29, No. 10, pp.1212-1219, Oct. 1994.

[4] S. Mitra, R. A. Rutenbar, L. R. Carley, and D. J. Allstot, "Substrate-Aware Mixed-Signal Macrocell Placement in WRIGHT," *IEEE J. Solid-State Circuits*, Vol. 30, No. 3, pp. 269-278, Mar. 1995.

[5] N. K. Verghese and D. J. Allstot, "Computer-Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits," *IEEE J. Solid-State Circuits*, Vol. 33, No. 3, pp. 314-323, Mar. 1998.

[6] J. Briaire and K. S. Krisch, "Substrate Injection and Crosstalk in CMOS Circuits," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1999, pp. 483-486.

[7] E. Charbon, P. Miliozzi, L. P. Carloni, A. Ferrari, and A. Sangiovanni-Vincentelli, "Modeling Digital Substrate Noise Injection in Mixed-Signal IC's," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 3, pp. 301-310, Mar. 1999.

[8] B. R. Stanisic, N. K. Verghese, R. A. Rutenbar, L. R. Carley, and D. J. Allstot, "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis," *IEEE J. Solid-State Circuits*, Vol. 29, No. 3, pp. 226-238, Mar. 1994.

[9] L. T. Pillage and R. A. Rohler, "Asymptotic Waveform Evaluation for Timing Analysis," *IEEE Trans. on Computer-Aided Design*, Vol. 9, No. 4, pp. 352-366, Apr. 1993.

[10] E. Chiprout and M. S. Nakhla, "Asymptotic Waveform Evaluation and Moment Matching for Interconnect Analysis," Kluwer Academic Publishers, 1994.

[11] S. Mitra, R. A. Rutenbar, L. R. Carley, and D. J. Allstot, "A Methodology for Rapid Estimation of Substrate-Coupled Switching Noise," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1995, pp. 129-132.

[12] M. K. Mayes and S. W. Chin, "All Verilog Mixed-Signal Simulator with Analog Behavioral and Noise Models," in *Symp. on VLSI Circuits Dig. Tech. Papers*, June 1996, pp. 186-187.

[13] M. Nagata and A. Iwata, "A Macroscopic Substrate Noise Model for Full Chip Mixed-Signal Design Verification," in *Symp. on VLSI Circuits Dig. Tech. Papers*, June 1997, pp. 37-38.

[14] M. Nagata and A. Iwata, "Substrate Noise Simulation Techniques for Analog-Digital Mixed LSI Design," *IEICE Trans. Fundamentals*, Vol. E82-A, No. 2, pp. 271-278, Feb. 1999.

[15] M. Nagata, Y. Kashima, D. Tamura, T. Morie, and A. Iwata, "Measurements and Analyses of Substrate Noise Waveform in Mixed Signal IC Environment," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1999, pp. 575-578.

[16] K. M. Fukuda, T. Kikuchi, T. Matsuura, and M. Hotta, "Measurement of Digital Noise in Mixed-Signal Integrated Circuits," *IEEE J. Solid-State Circuits*, Vol. 30, No. 2, pp. 87-92, Feb. 1995.

[17] K. M. Fukuda, T. Anbo, T. Tsukada, T. Matsuura, and M. Hotta, "Voltage-Comparator-Based Measurement of Equivalently Sampled Substrate Noise Waveforms in Mixed-Signal Integrated Circuits," *IEEE J. Solid-State Circuits*, Vol. 31, No. 5, pp. 726-731, May. 1996.

[18] T. J. Gabara, W. C. Fischer, J. Harrington, and W. W. Troutman, "Forming Damped LRC Parasitic Circuits in Simultaneously Switched CMOS Output Buffers," *IEEE J. Solid-State Circuits*, Vol. 32, No. 3, pp. 407-418, Mar. 1997.

[19] M. Ingels and M. S. J. Steyaert, "Design Strategies and Decoupling Techniques for Reducing the Effects of Electrical Interference in Mixed-Mode IC's," *IEEE J. Solid-State Circuits*, Vol. 32, No. 7, pp. 1136-1141, Jul. 1997.

[20] P. Larsson, "Power Supply Noise in Future IC's: A Crystal Ball Reading," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1999, pp. 467-474.

[21] T. A. Johnson, R. W. Knepper, V. Marcello, and W. Wang, "Chip Substrate Resistance Modeling Technique for Integrated Circuit Design," *IEEE Trans. on Computer-Aided Design*, Vol. CAD-3, No. 2, pp. 126-134, Apr. 1984.

[22] I. L. Wemple and A. T. Yang, "Integrated Circuit Substrate Coupling Models Based on Voronoi Tessellation," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, pp. 1459-1469, Dec. 1995.

[23] N. K. Verghese, D. J. Allstot and M. A. Wolfe, "Verification Techniques for Substrate Coupling and Their Application to Mixed-Signal IC Design," *IEEE J. Solid-State Circuits*, Vol. 31, No. 3, pp. 354-365, Mar. 1996.

[24] E. Charbon, R. Gharpurey, R. G. Meyer, and A. Sangiovanni-Vincentelli, "Substrate Optimization Based on Semi-Analytical Techniques," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 2, pp. 172-190, Feb. 1999.

[25] R. Gharpurey and R. G. Meyer, "Modeling and Analysis of Substrate Coupling in Integrated Circuits," *IEEE J. Solid-State Circuits*, Vol. 31, No. 3, pp. 344-353, Mar. 1996.

[26] R. Singh, "A Review of Substrate Coupling Issues and Modeling Strategies," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1999, pp. 491-498.

[27] T. Blalack and B. A. Wooley, "The Effects of Switching Noise on an Oversampling A/D Converter," in *ISSCC Dig. Tech. Papers*, Feb. 1995 , pp. 200-201.