A 12b 50 MHz 3.3 V CMOS Acquisition Time Minimized A/D Converter

Young-Deuk Jeon*, Byeong-Lyeol Jeon**, Seung-Chul Lee*, Sang-Min Yoo*,
and Seung-Hoon Lee*

*Dept. of Electronics Engineering, Sogang University, Seoul, Korea
**Hyundai Electronics Industries Co., Ltd., Ichon, Korea
TEL: +82-2-705-8471, FAX: +82-2-706-4216, e-mail: hoonlee@ccs.sogang.ac.kr

Abstract- A 12b 50 MHz CMOS analog-to-digital converter (ADC) based on a pipelined architecture was designed to demonstrate acquisition time minimization techniques for high-speed two-stage amplifiers. The proposed techniques reduce overshoots and undershoots of amplifier outputs and acquisition time by controlling the bias currents of amplifiers. The prototype ADC was fabricated in a 0.35 um double-poly triple-metal n-well CMOS technology. The measured signal-to-noise-and-distortion ratio is improved by more than 5 dB using the proposed techniques at a 50 MHz clock. The ADC power consumption is 200 mW at 3.3 V and 50 MHz.

I. INTRODUCTION

The rapid advances of high-speed digital signal processing applications such as digital camcorders, medical imaging equipments, and portable data communications have created the need for high-speed, high-resolution analog-to-digital converters (ADCs).

For high-speed applications, flash ADCs typically achieve the highest conversion rate. However, for more than 8b resolution, flash ADCs suffer from the exponential growth of die area and power dissipation. Pipelined ADCs which achieve 10b to 12b resolution at a high conversion rate have been proposed to solve these problems [1]-[5]. However, ADCs based on bipolar and BiCMOS technologies have drawbacks in large power dissipation, large chip area, and incompatibility with CMOS on-chip digital circuits. While CMOS ADCs could solve the problems partially, the conversion speed has been limited due to the finite bandwidth of residue amplifiers needed in pipelined ADCs.

In this work, acquisition time minimization techniques are proposed to realize high-speed two-stage amplifiers with little modification of the conventional system architecture. The proposed techniques reduce the acquisition time of amplifiers and the overshoots and undershoots of amplifier outputs. As a test vehicle for the proposed techniques, a fully differential 12b 50 MHz ADC was fabricated in a 0.35 um CMOS process.

II. ACQUISITION TIME MINIMIZATION TECHNIQUES

In pipelined ADCs, the single-bit-per-stage design is conventionally chosen to maximize interstage bandwidth and to minimize required residue amplifier settling time. However, the design method increases hardware and power dissipation since the required stages are increased in high-resolution ADCs [6]. As a result, for more than 12b ADCs, the multibit-per-stage design is recommendable to optimize chip area and power dissipation.

The proposed techniques reduce the settling time by varying the -3dB bandwidth (f_{-3dB}) and the phase margin (ϕ_{PM}) of the interstage residue amplifiers.

A. Principle

The output waveform and simple block diagram of a typical two-stage amplifier are shown in Fig. 1. The acquisition time ($t_{acquisition}$) of the amplifier in Fig. 1 (a) is given by

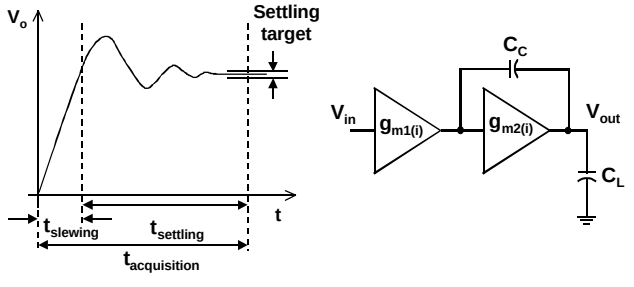
$$t_{acquisition} = t_{slewing} + t_{settling} \quad (1)$$

where $t_{slewing}$ is the slewing time it takes for the amplifier output to slew toward the targeted value, and $t_{settling}$ is the settling time it takes for the amplifier output to settle within a specified amount of the targeted value after slewing. In the two-stage amplifier in Fig. 1 (b), the slewing and settling time can be reduced by improving the f_{-3dB} and ϕ_{PM}, respectively. Then, the f_{-3dB} and ϕ_{PM} are approximately correlated as follows :

$$f_{-3dB} \mu g_{m1} / C_C \quad (2)$$

$$f_{PM} = 90° - tan^{-1}((g_{m1} / C_C) * (C_L / g_{m2})) \quad (3)$$

where g_{m1} and g_{m2} are the transconductances of the first and second stage amplifiers, C_C is the compensation capacitor, and C_L is the load capacitor. In the conventional circuits, both of the f_{-3dB} and ϕ_{PM} can not be improved simultaneously due to the (g_{m1}/C_C) term.



(a) (b)

Fig. 1. Typical two-stage amplifier : (a) output waveform and (b) block diagram.

TABLE I
Acquisition Time Minimization Techniques.

	Slewing period	Settling period
HSM*1	$g_{m1} > g_{m1(i)}$ $g_{m2} = g_{m2(i)}$	$g_{m1} = g_{m1(i)}$ $g_{m2} < g_{m2(i)}$
HSM*2	$C_C < C_{C(i)}$	$C_C > C_{C(i)}$

(*HSM: High-Speed Mode)

The proposed techniques improve the f_{-3dB} and ϕ_{PM} by varying the g_m and C_C during the slewing and settling period. For example, from (2) and (3), the f_{-3dB} is improved by increasing the g_{m1} or by decreasing the C_C during the slewing period and the ϕ_{PM} is improved by increasing the g_{m2} and C_C or by reducing the g_{m1} during the settling period. The results are summarized in Table I where the $g_{m(i)}$ and $C_{C(i)}$ represent the transconductance and compensation capacitor of the conventional two-stage amplifier and indicate the initial values before the g_m and C_C change. The high-speed mode 1 (HSM1) controls the g_m and the high-speed mode 2 (HSM2) controls the C_C to improve the f_{-3dB} and ϕ_{PM} in the amplification phase, simultaneously. Both of the HSM1 and HSM2 minimize the amplifier acquisition time with little additive power consumption. However, since the HSM2 needs complex switches to control C_C and generates parasitic poles related to the resistors and capacitors of MOS switches, it is difficult to implement the circuit. As results, the HSM1 is adopted in this work due to the relatively simple circuit implementation.

B. Circuit Implementation

The HSM1 based on the g_m-control technique is implemented in Fig. 2 and Fig. 3. A fully differential folded-cascode amplifier with a dynamic common-mode feedback circuit (CMFB) is shown in Fig. 2, which is the first-stage amplifier of the two-stage amplifier. Transistors, M1 to M3, form an input stage determining the g_{m1}. The output stage composed of M4 to M11 adopts the cascode architecture to achieve the high gain. The bias circuit (AMP BIAS) supplies bias voltages for the amplifier.

The g_m-control technique is operated as follows. Since the g_m of the input pair M1 and M2 operating in strong inversion is proportional to the square root of its drain current, the g_m is changed by the tail current of the input pair. The drain current of M3 is easily controlled by BIAS4. The increasing tail current, however, reduces drain currents of output transistors, M6 and M7, if and only if drain currents of M4 and M5 are fixed.

When a large differential input signal is applied to the input pair of the amplifier, output transistors, M6 or M7, may not operate temporarily in the saturation region caused by reduced currents. As results, drain currents of M4 and M5 need to be also increased with the increased drain current of M3 to maintain the constant current in the output stage for high-speed operation. It means that BIAS4 needs to be increased at the same time BIAS1 is decreased.

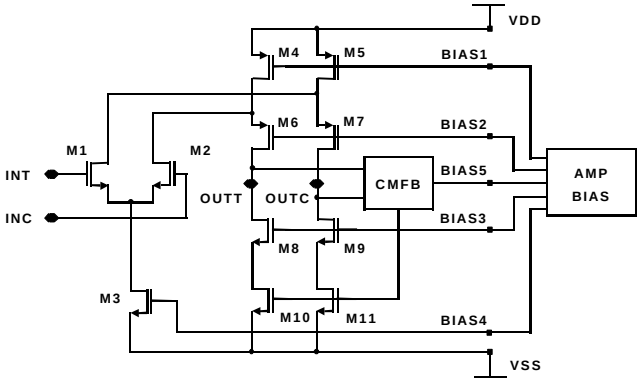


Fig. 2. First stage amplifier.

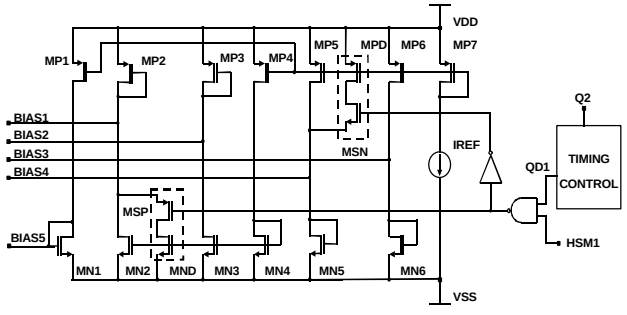


Fig. 3. Proposed bias circuit.

The g_m-control circuit is implemented by means of two current switches, MSN and MSP, and two current mirrors, MND and MPD, with little area overhead as shown in Fig. 3. Transistors, MPD and MSN are connected to the drain and source of MP5 in parallel. When MSN is turned on, the drain current of MPD is added to the bias current of MN5 and increases BIAS4 with the drain current of M3 in Fig. 2. The BIAS1 is also controlled in the same way. The g_m ratio, which is not so sensitive in real conversion process, is adjusted by the sizes of MND and MPD, which are about 20 % of that of MN2 and MP5 in the proposed bias circuit, respectively.

The control signal, QD1, to increase g_m, is internally generated by the timing control block and the mode control, HSM1, is externally connected to demonstrate the proposed technique. When HSM1 is low, the amplifier operates in a normal mode, and MSN and MSP are turned off. On the other hand, when HSM1 is high, the amplifier operates in a high-speed mode. The timing control circuit is shown in Fig. 4. When Q2 of the amplification clock phase is high, QD1 is high during the slewing period and is low during the settling period. The high duration of QD1 is adjusted by the inverter gate delay time and the capacitors, CD1 and CD2, of the delay generation block, corresponding to about 30 % of Q2 in the proposed circuit. Although the slewing period is increased or decreased by about 40 % due to process variations, the acquisition time is not critically affected.

C. Simulation Results

The two-stage amplifiers of the ADC based on the proposed

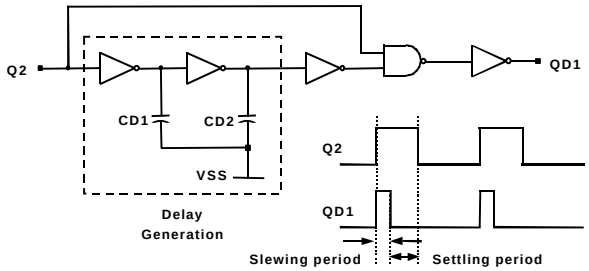


Fig. 4. Timing control circuit.

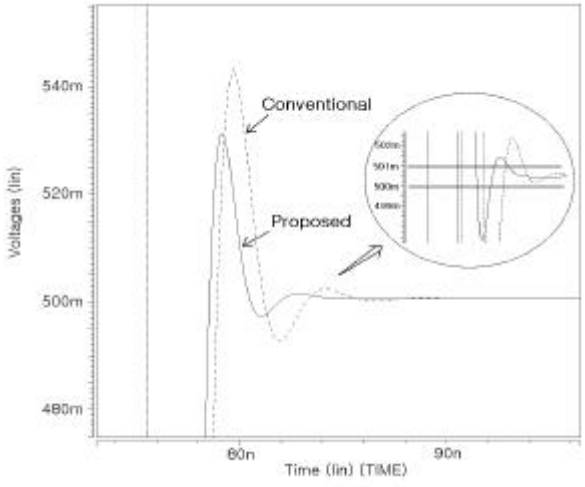


Fig. 5. Transient responses of the two-stage amplifier.

technique were simulated in a 0.35 um double-poly triple-metal n-well CMOS technology. The transient responses by the conventional circuit and the proposed circuit are shown in Fig. 5 and compared using an identical architecture. The acquisition time of the amplifier is 8.8 ns in the proposed circuit. It is about 10 % faster than 9.7 ns in the conventional circuit without amplifier modifications.

III. Prototype ADC Based On The Proposed Technique

The block diagram of the proposed 3.3 V 12b pipelined ADC is illustrated in Fig. 6, based on a conventional four-stage pipelined architecture. The ADC consists of an input sample-and-hold amplifier (SHA), three 4b multiplying digital-to-analog converters (MDACs), four 4b subranging flash ADCs, a self-bias generator, digital correction logic, and a clock generator. Two non-overlapping clock phases, Q1 and Q2, are internally generated for concurrent operations of all stages to convert an analog input signal to a digital output code. The proposed acquisition minimization technique is applied to three MDACs based on a two-stage amplifier. Each stage generates a 4b digital code from each flash ADC and the 4b digital code is stored in the digital correction logic. The interstage offset and clock feed-through errors are digitally corrected in the digital correction logic by overlapping one bit in each stage except the last. As a result, a final 13b digital code is obtained. The ADC

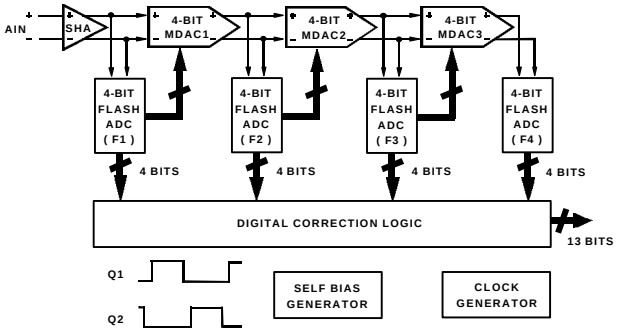


Fig. 6. Block diagram of the proposed ADC.

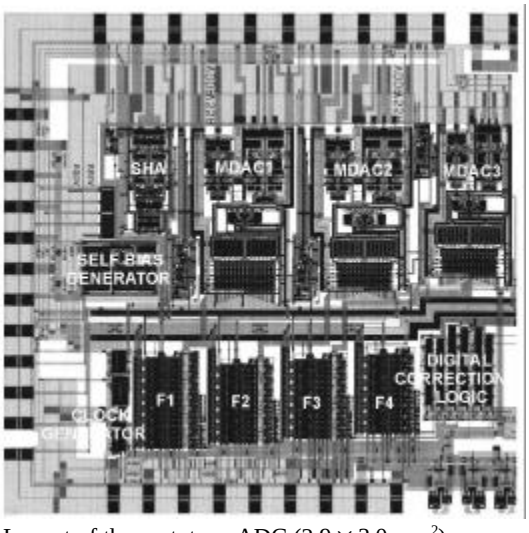


Fig. 7. Layout of the prototype ADC (2.9×3.0 mm^2).

system employs a fully differential architecture in analog signal paths to reduce noise.

IV. Experimental Results

The prototype ADC was fabricated in a 0.35 um double-poly triple-metal n-well CMOS technology. The ADC was laid out as shown in Fig. 7 and the active die area is 8.7 mm^2 (= 2.9×3.0 mm^2). The measured differential and integral nonlinearities (DNL and INL) are plotted in Fig. 8. The largest DNL is less than 0.6 LSB at a 12b accuracy, but the largest INL shows 2.2 LSB level due to the limited matching properties of the MDAC1 capacitors. The INL can be improved further by a more careful layout technique and by employing larger unit capacitors in the MDAC1. It is noted that, currently, the process itself is being developed.

The proposed technique is demonstrated in Fig. 9, showing the measured signal-to-noise-and-distortion ratio (SNDR) versus sampling frequency before and after the proposed high-speed mode, where the input frequency is kept constant at 1 MHz. It is observed that the SNDR at 50 MHz is improved from 51 dB to 56 dB after the high-speed mode engaged. It is feasible to make higher speed ADCs with CMOS technologies based on the proposed technique.

The SNDR is closely matched to the theoretical value, which is obtained by roughly subtracting 13 dB from the ideal SNDR 74 dB for 12b, due to the 2.2 LSB level of INL. The coupled input noise from the test boards and the low-performance signal sources also degraded the SNDR performance of the prototype ADC at high input frequencies. With the proposed technique, about 95 % of the blind-assembled 40 samples are working within the speed specification. The power consumption of the prototype ADC was measured to be 200 mW with a 50 MHz clock and at 3.3 V. The typical measured performance of the prototype ADC is in Table II.

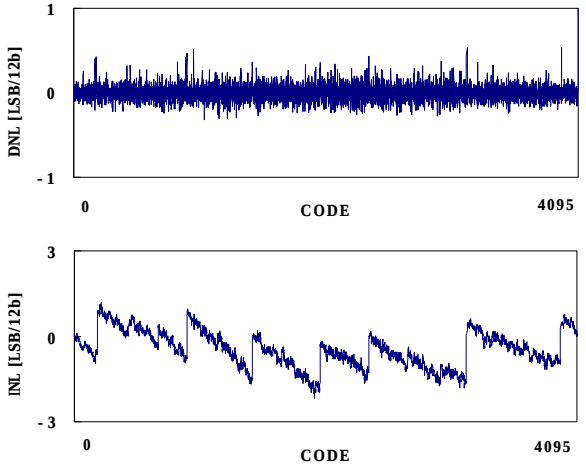


Fig. 8. Measured DNL and INL.

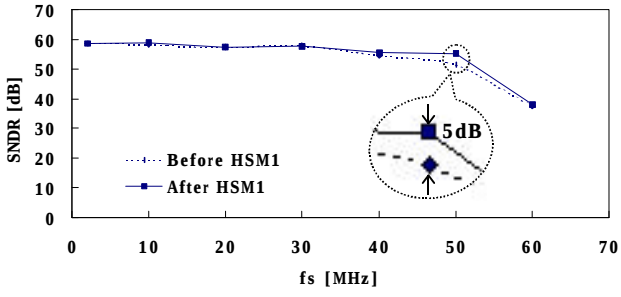


Fig. 9. SNDR versus sampling frequency (fin = 1 MHz).

TABLE II
Typical Measured Performance of The Prototype ADC.

Resolution	12 bits
Supply Voltage	3.3 V
Conversion Rate	50 MHz
Power	200 mW
DNL	± 0.7 LSB
INL	± 2.3 LSB
Input Range	2.8 Vp-p
Active Die Area	2.9×3.0 mm^2
Technology	0.35 um n-well CMOS

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