Design Challenges for 0.1um and Beyond

Takayasu Sakurai

Center for Collaborative Research
University of Tokyo
Tokyo, Japan, 106-8558
Tel : +81-3-3402-6226
Fax : +81-3-3402-6227
e-mail: tsakurai@iis.u-tokyo.ac.jp

Abstract - If we look into the scaling law carefully, we find that three crises can be stringent in realizing LSI's for 0.1um and beyond: namely power crisis, interconnection crisis, and complexity crisis. This paper describes these crises and possible solutions to cope with the problems.

Summary

If we look into the scaling law carefully, we find that three crises can be stringent in realizing LSI's for 0.1um and beyond: namely power crisis, interconnection crisis, and complexity crisis.

As for power crisis, there are activities to lower the power consumption from device level, circuit level to system level. Lowering supply voltage (V_{DD}) is very effective in reducing the power but the threshold voltage (V_{TH}) should be reduced at the same time for high-speed operation. The low VTH, however, increases the leakage current. To overcome this situation, V_{TH} and V_{DD} control through the use of multiple V_{TH}, variable V_{TH}, multiple V_{DD} and variable V_{DD} are intensively pursued and some have been productized. At the system level, system LSI approach is promising for realizing low power and the new trend is to exploit cooperation of software and hardware. In the sub 1-volt design, watch out for the abnormal temperature dependence of drain current.

The interconnection will be determining cost, delay, power, reliability and turn-around time of the future LSI's rather than MOSFET's. RC delay problem can be solved through LSI architecture realizing "the further, the less communication" with the help of local memories.

It is just impossible to design LSI's with 100 million transistors from scratch. The complexity issue can only be solved by the sharing and re-use of design data. So-called IP-based design will be preferable. The virtual components are put together on a silicon to build billion transistor LSI's, which can be compared to the present system implementation with pre-manufactured LSI components.

References

[1] T.Sakurai Ed., "Low-power high-speed LSI design & technology," Realize publishing company, ISBN4-89808-004-9 C3055 ¥56000E, Phone: +81-3-3815-8511.

[2] T.Sakurai Ed., "System LSI – Applications and Technology," Science Forum publishing, ISBN4-916164-30-X C3000 ¥48000E, Phone: +81-3-5689-5611

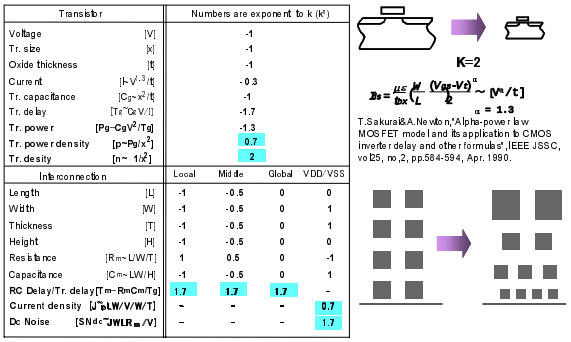


Fig.1 Scaling Law

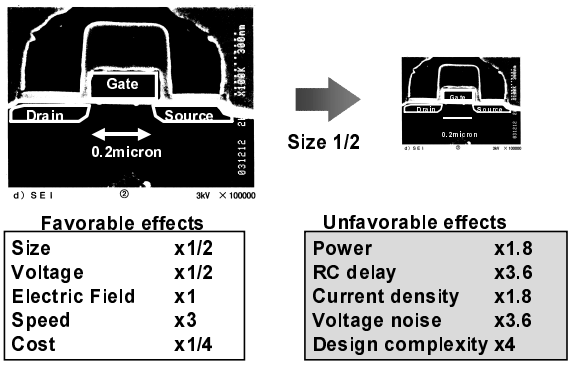


Fig.2 Scaling Law

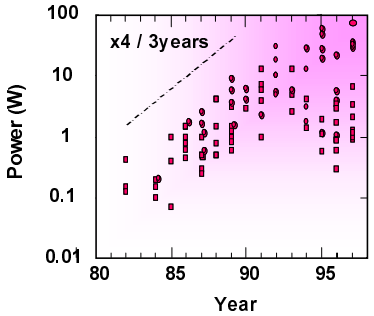


Fig.3 Ever Increasing VLSI Power

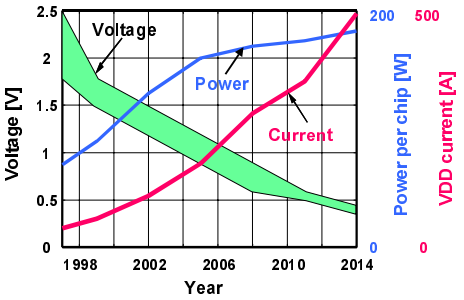


Fig.4 VDD, Power and Current Trend (From SIA)

Power range	Concerns	Typical applications (All need high-perf.)
< 0.1W	· Battery life	Portable · PDA · Communications
~ 1W	· Inexpensive package limit · System heat (10W / box)	Consumer · Set-Top-Box · Audio-Visual
> 10W	· Ceramic package limit · IR drop of power lines	Processor · High-end MPU's · Multimedia DSP's

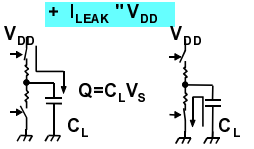
Fig.5 Necessity for Low-Power Design

- NMOS ⇒ CMOS
  Cost up
- Bipolar ⇒ CMOS
  Speed down
- Not cost nor speed but power set the technology trend.
- Integration can achieve low cost and high speed as a system.

Fig.6 What sets the technology trend?

$$P = \alpha \cdot C_L \cdot V_S \cdot V_{DD} \cdot f_{CLK} + \alpha \cdot I_{SC} \cdot \Delta t_{SC} \cdot V_{DD} \cdot f_{CLK} + I_{DC} \cdot V_{DD} + I_{LEAK} \cdot V_{DD}$$

Charging & discharging
Crowbar current
Static current
Subthreshold leak current



α : Switching probability
C_L : Load capacitance
V_S : Signal swing
V_{DD} : Supply voltage
I_{SC} : Mean crowbar current
Δt_{SC} : Crowbar current duration
f_{CLK} : Clock frequency
I_{DC} : DC current
I_{LEAK} : Subthreshold leak current

$C_L \cdot V_S$ amount of charge loses V_{DD} of potential
-> $C_L \cdot V_{DD} \cdot V_S$ energy consumption per cycle

Fig.7 Expression for CMOS Power

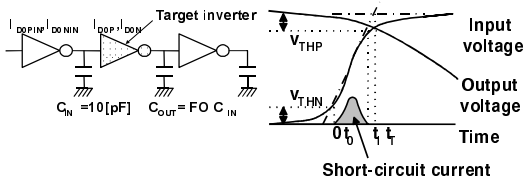


Fig.8 Voltage waveform of CMOS inverter

$$P_S = \frac{k(v_{D0P})\, fo_P^2 C_{IN} V_{DD}^2}{\frac{v_{D0P} g(v_T,\alpha)}{2k(v_{D0P})} FO\beta_r + h(v_T,\alpha) fo_P}$$

$$g(v_T,\alpha) = \frac{\alpha_N + 1}{f(\alpha)} \frac{(1-v_{TN})^{\alpha_N} (1-v_{TP})^{\alpha_P/2}}{(1-v_{TN}-v_{TP})^{\alpha_P/2+\alpha_N+2}} \qquad FO = \frac{C_{OUT}}{C_{IN}} \text{ (Fanout)}$$

$$h(v_T,\alpha) = 2^{\alpha_P}(\alpha_P+1) \frac{(1-v_{TP})^{\alpha_P}}{(1-v_{TN}-v_{TP})^{\alpha_P+1}}$$

$$k(v_{D0P}) = \frac{0.9}{0.8} + \frac{v_{D0P}}{0.8} \ln\frac{10 v_{D0P}}{e} \qquad fo_P = \frac{I_{D0P}}{I_{D0PIN}} \quad \beta_r = \frac{I_{D0P}}{I_{D0N}}$$

K. Nose and T. Sakurai, "Closed-Form Expressions for Short-Circuit Power of Short-Channel CMOS Gates and Its Scaling Characteristics," ITC-CSCC (Korea), July 1998.

Fig.9 Short-circuit power dissipation formula

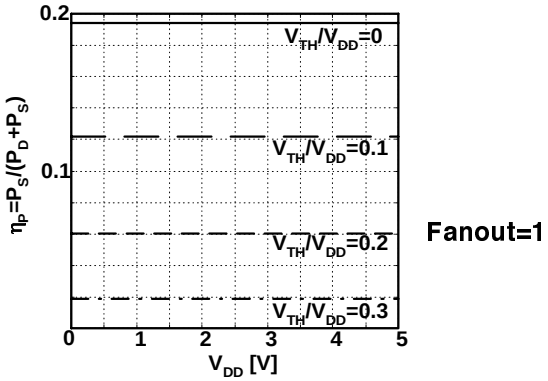
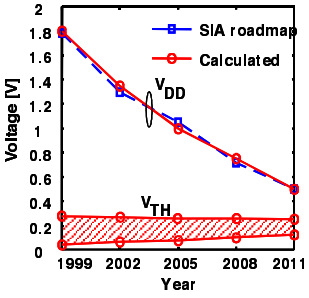


Fig.10The change of the short-circuit power dissipation with scaling



Koichi Nose and Takayasu Sakurai, "Optimization of VDD and VTH for Low-Power and High-Speed Applications", ASPDAC'00, A6.1, Jan. 2000.

Fig.11 VDD, VTH, Power and Current Trend

P = α *f* C Vs V_{DD} + leakage(sub-Vth,gate,D/S)

Low-voltage
- Variable-V_{TH}, multi-V_{TH}
  (Super-Cut-off CMOS, dynamic leakage cut-off SRAM, positive temp. coeff., d-type CMOS, optimum voltages)
- Variable-V_{DD}, multi-V_{DD}
  (Software control)

Low-swing
- Bus, clock, interconnection
  (Reduced Clock Swing F/F, bus with sense-amp. F/F, low-power repeater insertion)

Others
- Easy library generation for early adoption of new tech.

Fig.12 Solving power issues

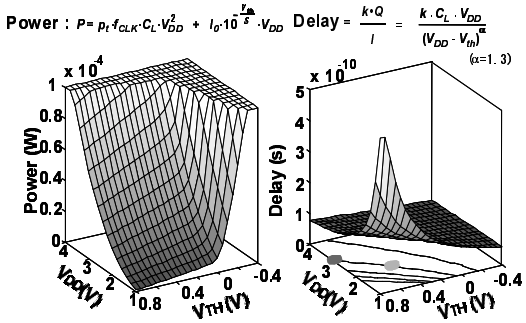


Fig.13 Power and delay

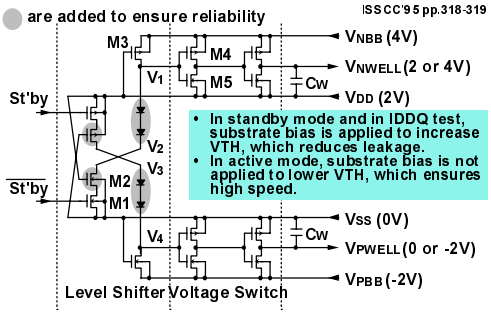


Fig.14 Standby Power Reduction (SPR) Circuit

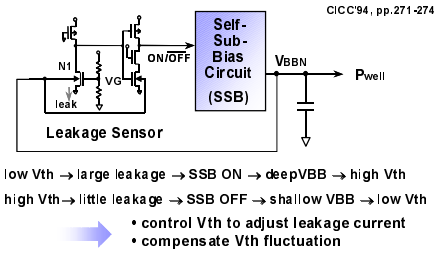


Fig.15 Self-Adjusting Threshold-voltage Scheme

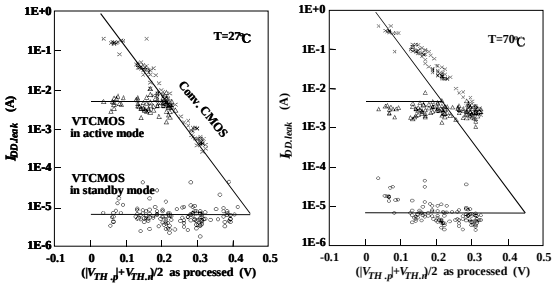


Fig.16 Measured I_{leak} in SAT+SPR

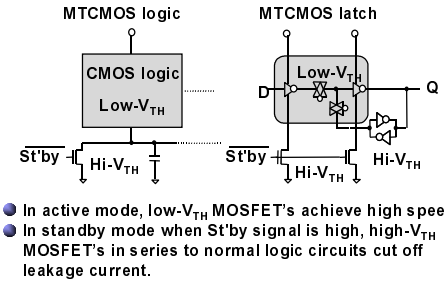


Fig.17 Multi-Threshold CMOS Circuit

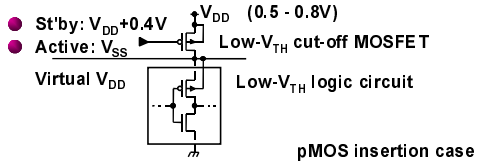


Fig.18 Super Cut-off CMOS (SCCMOS). H.Kawaguchi and K.Nose, T.Sakurai, "A CMOS Scheme for 0.5V Supply Voltage with pico-Ampere Standby Current," ISSCC, pp.192-193, Feb. 1998.

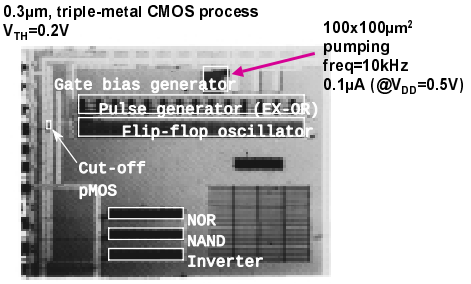


Fig.19 Super Cut-off CMOS Scheme (SCCMOS)

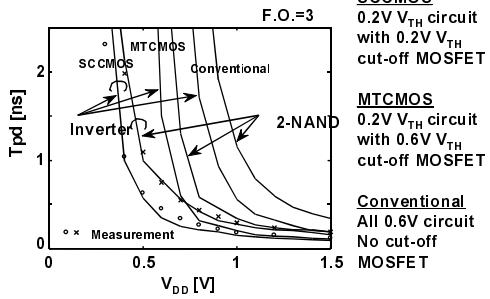


Fig.20 Delay characteristics (inverter & NAND)

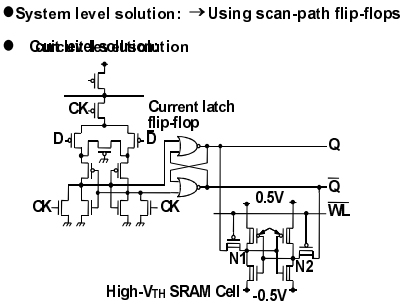


Fig.21 Losing information in standby

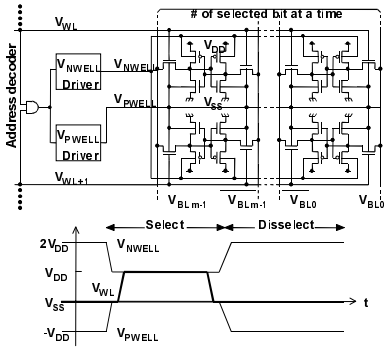


Fig.22 Dynamic Leakage Cut-off

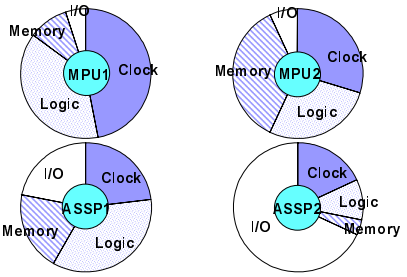
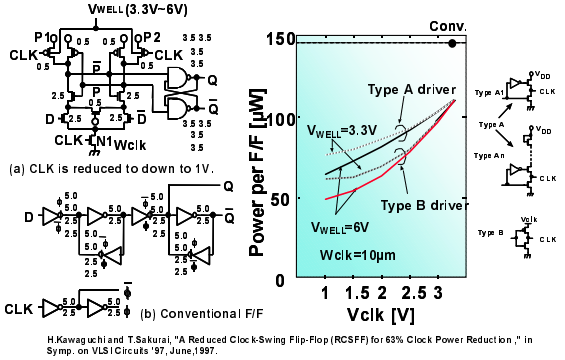


Fig.23 Power Distribution in CMOS LSI's



H.Kawaguchi and T.Sakurai, "A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Clock Power Reduction," in Symp. on VLSI Circuits '97, June,1997.

Fig.24 Reduced Clock Swing Flip-Flop

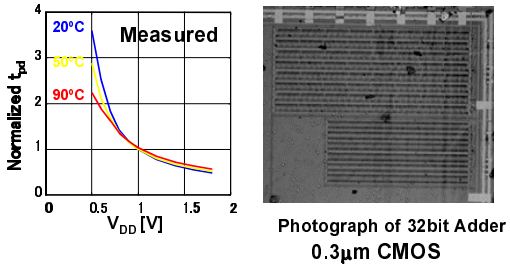


Fig.25 Positive temp. coeff. in low-voltage

• α-power law model (T = Temp. μ= Mobility)

$I_{DS} \propto \mu(T)\,(V_{DD} - V_{TH}(T))^{\alpha}$

	T ↗	T ↘
$\mu(T) = \mu(T_0)(T / T_0)^{-m}$	↘	↗
$V_{TH}(T) = V_{TH}(T_0) - \kappa(T - T_0)$	↘	↗

Typical Value : α=1.5, m=1.5, κ=2.5[mV/T]

Effects of V_{TH} and μ on I_{DS} when temp. goes up 100[K]

	V_{TH} effect	μ effect
V_{DD}=2.5V, V_{TH}=0.5V	10% ↗	35% ↘
V_{DD}=1.0V, V_{TH}=0.2V	55% ↗	35% ↘

Fig.26 Cause of positive temp. dependence of I_{DS}

Paper#	WP25.1	WP25.3	WP25.7	WP25.4
Company	IBM (East Fishkill)	IBM (Essex & Austin)	IBM (Rochester)	Samsung
Target	PowerPC 604e	PowerPC 750	PowerPC	Alpha
	32b	for Apple	64b	64b
PD/FD	PD	PD (SIMOX)	PD (SIMOX)	FD (SIMOX/Unibond no dep.)
Rule	0.25um		0.2um (Leff=0.12um)	0.25um
Interconnect	5 Al + Wlocal	Cu	6 Cu	4 Al
Area	49mm2		139mm2	209mm2
# of Tr's	6.5M		34M	9.7M
Freq.	500MHz	550MHz@85C, fast proc.	550MHz	600MHz
VDD	1.7V	2V	1.8V	1.5V (2V I/O)
Power		5.1W@2V,400MHz	24W	40W
Speed gain o	25-30%	20%	20%	30%@1.2V, 20%@1.5V SRAM
	22% Ctotal reduction	12% by Cj	15-20% simple gates	
	10-15% more Ids	15-25% by less body-bias	25-40% complex gates	

Fig.27 SOI Processors in ISSCC'99

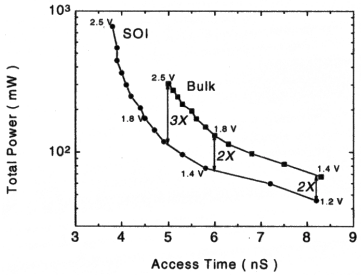


Fig.28Hi-Speed is Low-Power.
www.erniefernandez.com/html/soi.html

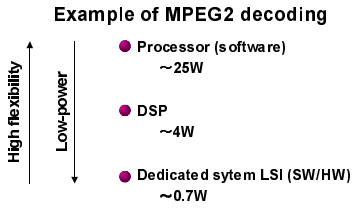


Fig.29 Approach to low-power LSI

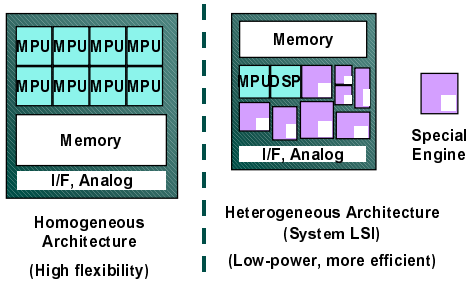
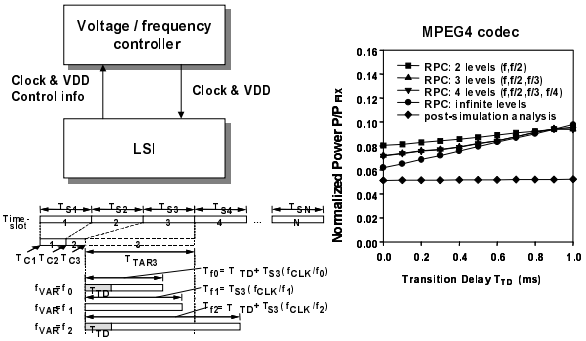
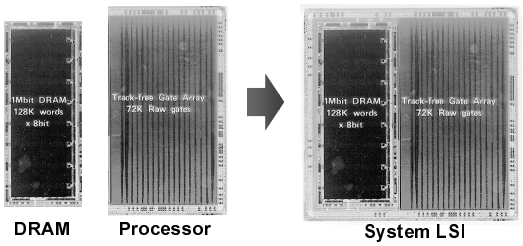


Fig.30 Homogeneous vs. Heterogeneous



Seongsoo Lee, T.Sakurai, "Run-time Power Control Scheme Using Software Feedback Loop for Low-Power Real-time Applications," ASPDAC'00, A5.2, Jan. 2000.

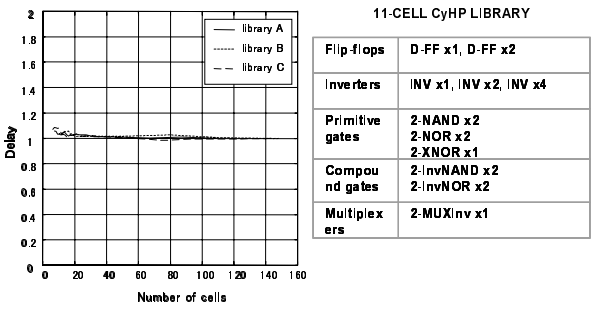
Fig.31 Software feedback loop for low-power



K.Sawada, T.Sakurai, et al, "A 72K CMOS Channelless Gate Array with Embedded 1Mbit Dynamic RAM," in Proc. CICC'88, pp.20.3.1-20.3.4, May 1988.

- Two orders of magnitude improvement in bandwidth and power

Fig.32 DRAM Embedding



11-CELL CyHP LIBRARY

Flip-flops	D-FF x1, D-FF x2
Inverters	INV x1, INV x2, INV x4
Primitive gates	2-NAND x2 2-NOR x2 2-XNOR x1
Compound gates	2-InvNAND x2 2-InvNOR x2
Multiplexers	2-MUXInv x1

N.Duc, T.Sakurai, "Compact yet High-Performance (CyHP) Library for Short Time-to-Market with New Technologies," ASPDAC'00, A6.2, Jan. 2000.

Fig.33Compact yet High-Performance (CyHP) Library for Low-Power Technologies

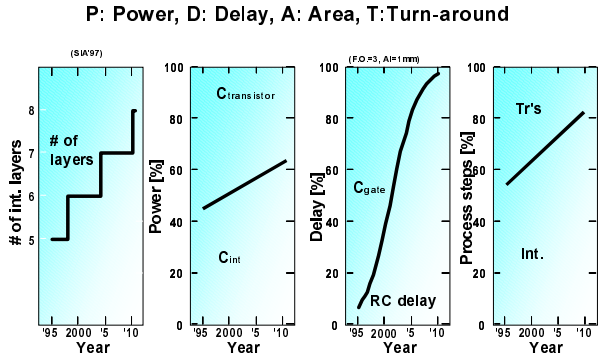


Fig.34 Interconnect determines cost & perf.

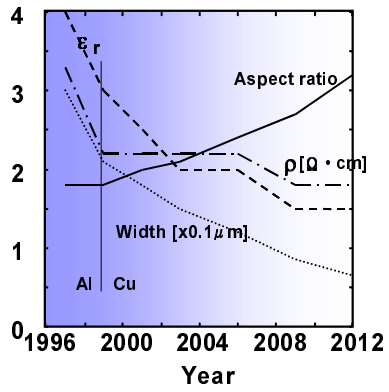


Fig.35 Interconnect parameters trends

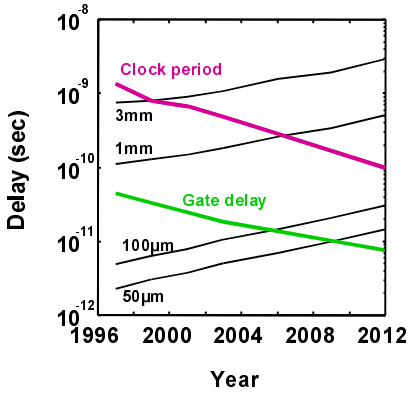


Fig.36 RC delay and gate delay

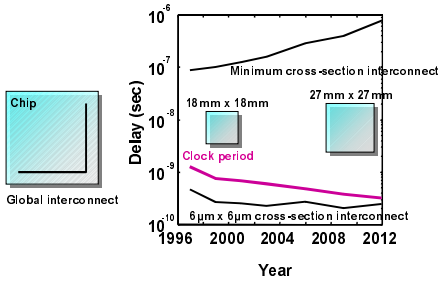


Fig.37 RC delay of global interconnections

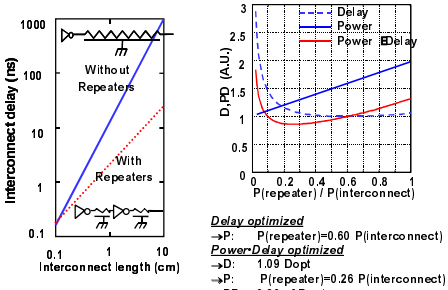


Fig.38 Delay and Power Optimization for Repeaters

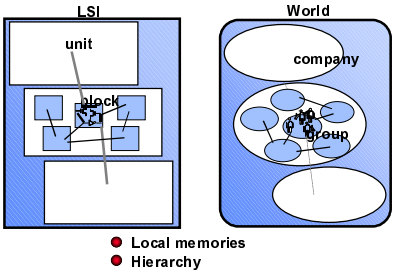


Fig.39 The further, the less

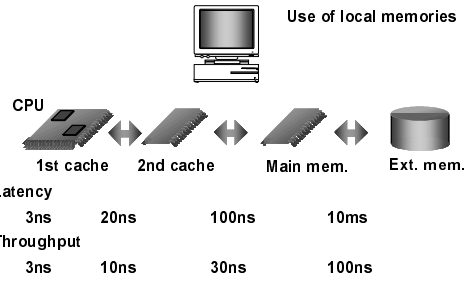


Fig.40 Locality in space & time

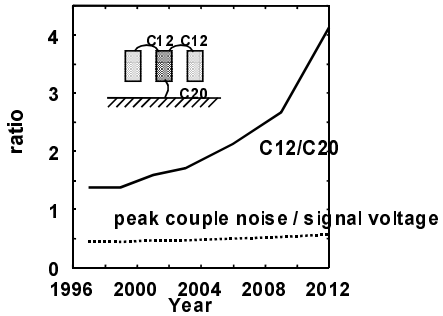
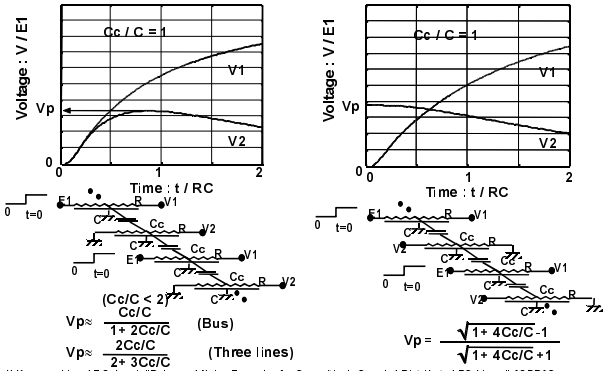
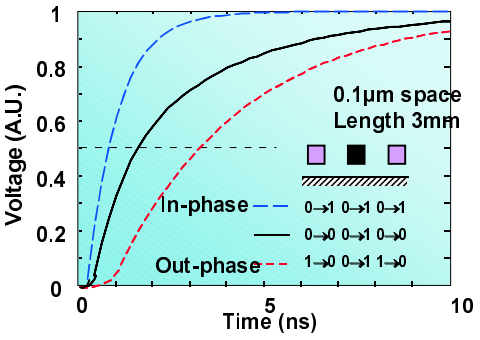


Fig.41 Capacitive Coupling Noise



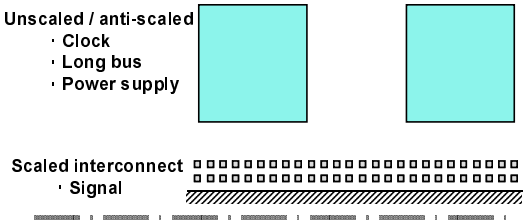
H.Kawaguchi and T.Sakurai, "Delay and Noise Formulas for Capacitively Coupled Distributed RC Lines," ASPDAC, Digest of Tech. Papers, pp35-43, Feb. 1998.

Fig.42 Coupling noise in RC bus



Difficulty in checking setup and hold time.

Fig.43 Coupling among Interconnection



1V 15W -> 15A current
5% noise -> 0.05V noise -> 3mΩ sheet R -> 10μm thick Al
Area pad + package, or thick layer on board is needed.

Fig.44 Interconnect Cross-Section and Noise

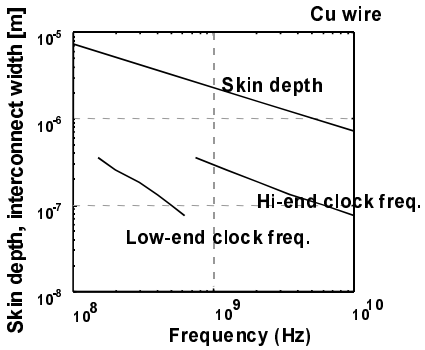


Fig.45 Skin Effects for Signal Lines

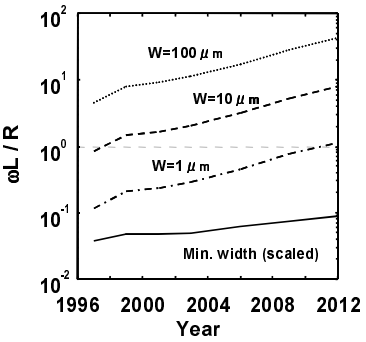


Fig.46 Inductive Effects

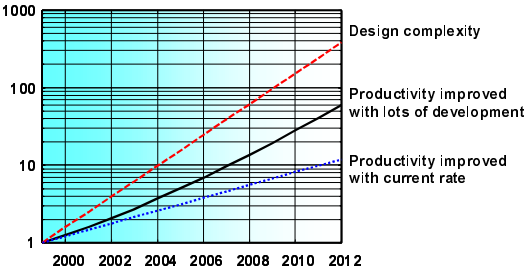


Fig.47 System LSI design complexity increases faster than productivity. (http://notes.sematech.org/97melec.htm)

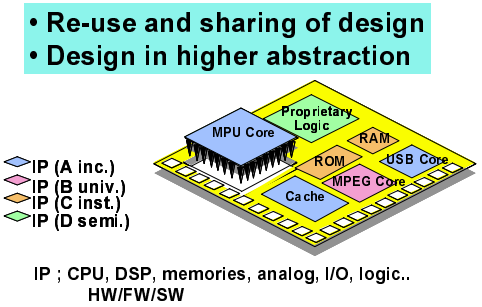
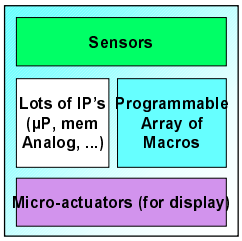


Fig.48. Overcome complexity crisis

Year	Unit	1999	2014	Factor
Design rule	μm	0.18	0.035	0.2
Tr. Density	/cm2	6.2M	390M	30
Chip size	mm2	340	900	2.6
Tr. Count per chip (μP)		21M	3.6G	170
DRAM capacity		1G	1T	256
Local clock on a chip	Hz	1.2G	17G	14
Global clock on a chip	Hz	1.2G	3.7G	3.1
Power	W	90	183	2.0
Supply voltage	V	1.5	0.37	0.2
Current	A	60	494.6	8
Interconnection levels		6	10	1.7
Mask count		22	28	1.3
Cost / tr. (packaged)	μcents	1735	22	0.01
Chip to board clock	Hz	500M	1.5G	3.0
# of package pins		810	2700	3.3
Package cost	cents/pin	1.61	0.75	0.5

Fig.49. LSI in 2014



- Sensors/actutors on chip
- 0.035μm 3.6G Si FET's with VTH & VDD control
- Locally synchronous 17GHz clock, globally asynchronous
- Chip / Package / Board system co-design

Fig.50 Chip in 2014