A Method for Linking Process-level Variability to System Performances

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Abstract— In this paper we present a statistical analysis method which bridges the statistical information between process-level and system-level. This enables us to evaluate the effect of process variation at the system level. Also, we can derive constraints on the process variation from a performance requirement. We show an example of the hierarchical statistical analysis applied to a Phase Locked Loop(PLL) circuit.

I. Introduction

Yield loss of VLSI caused by a variation of device characteristics has become a crucial problem. In order to overcome this problem, various researches in statistical circuit simulation and parametric yield optimization have been reported [1]. However, these researches mainly aim at block level circuit analysis, and system level statistical analysis have not been well studied. This is because statistical analysis needs a number of simulations so that the system level statistical simulation in a flat manner becomes practically infeasible.

In this paper we present a statistical analysis method which bridges the statistical information between process-level and system-level. System-level performance can be explicitly described by process-level physical parameters such as L_{d}, T_{ox} etc. Using this method, we can analyze the system-level performance variability with process variation. The simulation cost which is required to build the link between each level is less expensive, the system level statistical analysis can be practically performed.

The paper is structured as follows. In section II a concept of hierarchical statistical analysis is described, and two important modeling technique — intermediate model and response surface model — is illustrated. In section III we show an example of the hierarchical statistical analysis applied to a Phase Locked Loop(PLL) circuit of which system level simulation with SPICE is very expensive or practically infeasible. It is demonstrated that the proposed method could be used to derive constraints on the process variation from a performance requirement.

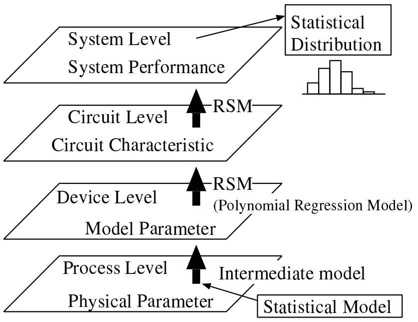

Fig. 1. Overview of hierarchical design for statistical analysis

II. Hierarchical statistical analysis

Performance variability of an LSI exists at various levels such as process, device, circuit, and system, which forms a hierarchy as shown in Fig. 1. Statistical analysis is performed to establish a relation between adjacent levels. For example, it is common to use device simulation to analyze the fluctuation of device characteristics due to process variations. The statistical behavior of the device is expressed, for example, as a set of worst/best case model parameters, which is then used in circuit simulation to produce a worst/best case circuit performance. In this way, we may obtain a worst/best case performance at the system level. However, this “one-level by one-level” approach cannot transform important statistical information such as correlation among performance parameters, and hence results in a poor statistical prediction. Also, we cannot see the effect of each physical parameter at the process level to the system performance.

It is important to transform statistical information at the process level up to the system level, which enables accurate performance modeling. By so doing, we can not only analyze the system-level performance variability but also derive constraints on the process variation from performance specifications. Our approach to this hierarchical statistical analysis is overviewed in Fig. 1. There are two important techniques. The first technique is a statistical device modeling which transforms the statistical information of the physical parameters to the model parameters [2]. The second technique is a hierarchical transformation of the statistical information from the device level up to the system level using response surface models [3, 4]. A response surface model (RSM) describes a performance parameter as a function of performance parameters of the lower level. Successive building of RSMs finally enables to express a system-level performance as a function of the physical parameters. We briefly describe these techniques below.

A. Statistical device modeling

Physical variations of a VLSI process are transfered to transistor model parameters by means of the concept of an intermediate model [2]. Statistical set of transistor model parameters is generated from the statistical information of the physical parameters at the process level. In this study, we use five parameters, L_{d}, W_{d}, K_{p}, N_{ch}, and R_{DS} as the physical statistical parameters. These parameters, say $\boldsymbol{y}$, are composed from non-correlated variables using Principal Component Analysis (PCA),

$$\boldsymbol{y} = \boldsymbol{U}\boldsymbol{\Lambda}^{1/2}\boldsymbol{x}, \tag{1}$$

where $\boldsymbol{U}$ is a matrix whose column vectors consist of eigenvectors of a correlation matrix of $\boldsymbol{y}$, and $\boldsymbol{\Lambda}$ is a matrix which has eigenvalues of the correlation matrix in diagonal.

B. Model-building of circuit and system levels

In the circuit and system levels, their characteristics are modeled as functions of performance characteristics of the lower level(RSM). We use first or second order polynomial functions for the RSM, and they are built by regression from simulated data.

The circuit characteristic z_i is expressed as a function of statistical process parameter $\boldsymbol{y}$ as follows,

$$z_i = f(\boldsymbol{y}) = b_0 + \sum_{i=1}^{N} b_i y_i + (\text{higher order terms}). \tag{2}$$

In the same way, RSM of the system level performance $\boldsymbol{r}$ can be modeled by the circuit performances at the circuit level.

$$\boldsymbol{r} = \boldsymbol{g}(\boldsymbol{z}) = \boldsymbol{g}(\boldsymbol{f}(\boldsymbol{y})) \equiv \boldsymbol{h}(\boldsymbol{y}). \tag{3}$$

Equation (3) expresses the relation between physical parameters and system performances. Using this equation, statistical information of the circuit performances can be acquired by those of the physical parameters.

As an example of utilizing the link between physical variables and system performances, a sensitivity analysis of system performances to physical parameters is presented. It should be noted that a sensitivity to correlated variable provides little information. For the purpose of sensitivity analysis to non-correlated variable, Eq. (3) is rewritten as a function of non-correlated variable $\boldsymbol{x}$ via Eq. (1),

$$\boldsymbol{r} = \boldsymbol{h}(\boldsymbol{U}\boldsymbol{\Lambda}^{1/2}\boldsymbol{x}) \equiv \boldsymbol{k}(\boldsymbol{x}). \tag{4}$$

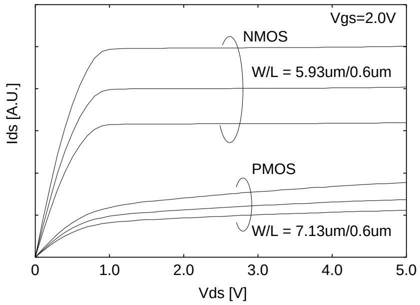

Fig. 2. CMOS I_{DS}-V_{DS} characteristics, typical case and 3σ worst-cases

After sensitive analysis to non-correlated variable using Eq. (4), the influence of physical parameter on system performances is evaluated by the following expansion of the sensitivity,

$$\frac{\partial r}{\partial x_i} = \sum_j \frac{\partial r}{\partial y_j} \cdot \frac{\partial y_j}{\partial x_i}. \tag{5}$$

Equation (5) indicates which physical parameter has dominant effect on the system performance.

III. EXPERIMENT

First we show I_{DS}-V_{DS} characteristics of a MOSFET used in the experiment. They are reproduced using an intermediate model and shown in Fig. 2 with 3σ worst-cases.

Phase Locked Loop (PLL) is selected as a test-vehicle of our methodology. The circuit consists of a phase frequency detector (PFD), a charge pump, a voltage control oscillator (VCO), and a frequency divider (Fig. 3). In order to perform a system level simulation, each block of the circuit is modeled using Verilog-A. For making the model, the source of variation needs to be taken into consideration and modeled as follows. As for the VCO, the relation of frequency to input voltage is approximated with a linear function. The sensitivity of the oscillation frequency with respect to the input voltage is represented by parameter k_{v}. As for the charge pump, the model is made using a constant current i_{ch} and a maximum input voltage which can supply it. When the input voltage does not exceed the maximum voltage, the charge pump supplies the constant current, and once the input voltage exceeds it, the output current decreases. So, the charge pump current is approximated by a piecewise linear function. As for the PFD, finite transition times for output rise and fall are modeled.

Before going into the examination of hierarchical statistical analysis with RSM, we first confirm the accuracy of the hierarchical performance analysis using the Verilog-A model. For this purpose, a hierarchical Monte Carlo analysis with the Verilog-A model is compared with a flat

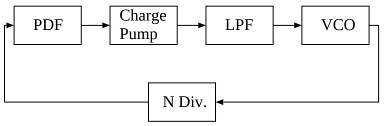

Fig. 3. PLL block diagram

Monte Carlo analysis based on SPICE simulation. We select lock up time as a system characteristic of the comparison. The procedure of the hierarchical Monte Carlo analysis with the Verilog-A models is as follows.

1. Monte Carlo analyses of circuit blocks are performed with Spice. Each parameter mentioned above is extracted for each set of random variables.
2. The lock up time of the whole system is analyzed with the Verilog-A models for each set of random variables using the extracted parameters in 1.

A flat Monte Carlo analysis is done with Spice using the same random variables as the hierarchical Monte Carlo analysis with the Verilog-A models. Due to high computational costs for a flat analysis with SPICE, the sample size of the Monte Carlo analysis is 100. If the behavioral modeling with Verilog-A preserves essential characteristics of the circuit operation, the result of the hierarchical analysis with the Verilog-A models results in a lock-up time close to that of the flat analysis with SPICE. In order to check this, a scatter plot of the hierarchical analysis with the Verilog-A model versus the flat analysis with Spice is shown in Fig. 4. Except for a few cases, reasonable agreement is achieved. The correlation coefficients between them is 0.888.

The source of discrepancies is explained as follows. A deviated sample is selected which is marked by a circle in Fig. 4. Figure 5 shows the lock-in behavior of this sample by both the hierarchical analysis with the Verilog-A models and the flat analysis with SPICE. Oscillation frequency is plotted as a function of time for each case. It can be said that the lock-in behavior is well modeled in the hierarchical analysis. It is revealed that the discrepancy comes from the definition of the lock up time. We define the lock up time as a time required to settle within 1 % of the target frequency. In this example, as seen in a magnified plot in Fig. 5, the second peak frequency by the hierarchical analysis is just a little above this threshold whereas that by the flat analysis is just a little below the threshold, which results in a fair amount of discrepancy in the lock up times. It is also confirmed that the lock-in behaviors of some other samples by the hierarchical analysis are consistent with those by the flat analysis with SPICE. We conclude that the hierarchical analysis with the Verilog-A models can simulate the lock-up behavior with reasonable accuracy.

Having confirmed the accuracy of the hierarchical analysis, we then build RSMs at the circuit level and the system level such that the physical parameters at the process level can be linked to the sub-circuit performances and then to the system performance. For this purpose, the following processes are done.

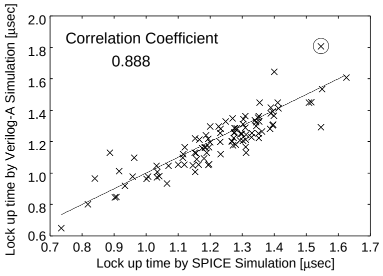

Fig. 4. Scatter plot between Spice and Verilog-A simulation

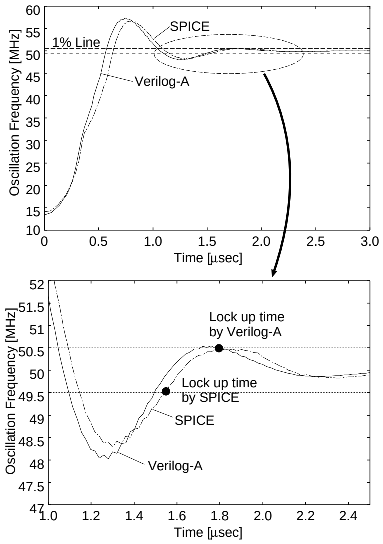

Fig. 5. Waveform of the lock on process in the Monte Carlo analysis

First, RSMs of sub-circuit characteristics are built at the circuit level. These RSMs are first order polynomials and confirmed that they had enough accuracy by the analysis of variance (ANOVA) [5]. As an example, the RSM of k_v is shown in Fig. 6.

Next, an RSM of a lock up time, which is a system level performance, is built by the same way as circuit level characteristics. In this case, the RSM is expressed as a function of sub-circuit characteristics, R and C of the low pass filter. A first order polynomial achieves a reasonable accuracy, which is verified by a multiple correlation coefficient R. In this experiment, $R = 0.968$, and it shows that the RSM approximates the system performance with enough accuracy. Fig. 7 shows the RSM of lock up time as the function of k_v of the VCO and R of the low pass filter.

Finally, substituting circuit-level RSMs into the

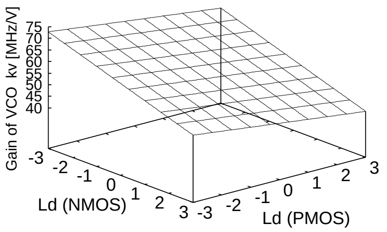

Fig. 6. RSM of k_v of the VCO versus L_d (NMOS) and L_d (PMOS) (Parameters are normalized by their means and standard deviations)

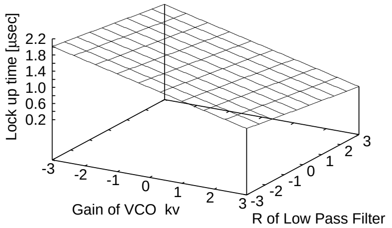

Fig. 7. RSM of the lock up time of the PLL (Parameters are normalized by their means and standard deviations)

system-level RSM, the lock up time is expressed as a function of process-level variations. For example, Fig. 8 shows the effect of L_d (NMOS) and R of the low pass filter to the lock up time characteristic. In this experiment, the simulation speed of the system level analysis with Verilog-A is about 100 times faster than the flat analysis with SPICE.

We show three applications of the hierarchical statistical analysis. One application is Monte Carlo analysis, another is worst-case analysis and the other is sensitivity analysis.

Monte Carlo analyses of this system performance are done with the RSM linking method. The same random variables are also used as in the previous Monte Carlo analyses with Spice and Verilog-A. The result of the Monte Carlo analysis with the proposed method is compared with ones with Spice and Verilog-A. It is assumed that R and C of the low pass filter are statistically independent and are normally distributed. The scatter plots between them is shown in Figs. 9 and 10.

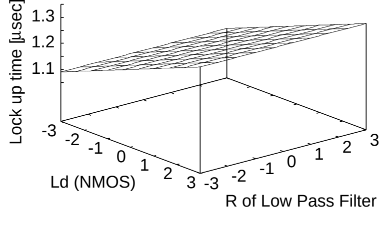

Fig. 8. RSM of lock range of PLL(Parameters are normalized by their means and standard deviations)

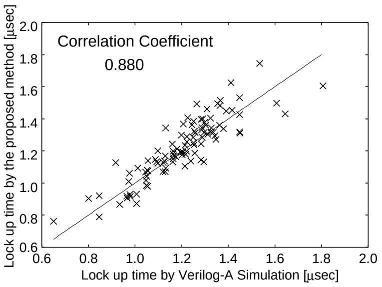

Fig. 9. Scatter plot between Verilog-A and the proposed method

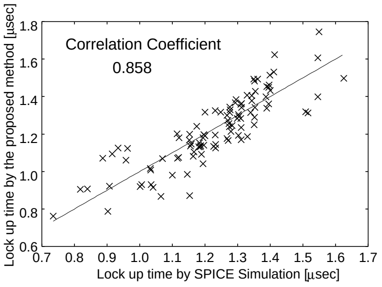

Fig. 10. Scatter plot between Spice and the proposed method

Although good accuracy is achieved in the RSMs both for the device level to the circuit level and for the circuit level to the system level, the scatter plot between Verilog-A and the proposed method (Fig. 9), which indicates the precision of the RSM, exposes a little inconsistency. The source of this error is considered that a little change in lock up behavior, such as shown in Fig. 5, gives large effect to the lock up time. However the correlation coefficient between them, 0.880, indicates good precision.

The scatter plot between Spice and the proposed method (Fig. 10) shows the total accuracy of our method. The correlation coefficient, 0.858, means that our method can link the physical level parameter to the system level parameter with good accuracy.

The worst-case analysis is described as the second application of the hierarchical statistical analysis as follows.

A histogram of the lock up time obtained by the flat Monte Carlo analysis with Spice simulation is shown in Fig. 11. The worst-case values are estimated by 3σ points from mean value of a 1000 samples Monte Carlo analysis using proposed RSM. These values are also plotted in Fig. 11 as "proposed method". The sample size of the flat Monte Carlo analysis shown in Fig. 11 is too small (100) to estimate the realistic worst-case. The worst-case values by the proposed method, however, indicate good agreement with the histogram of the flat Monte Carlo analysis.

In order to compare this worst-case analysis with a conventional worst-case analysis, the worst-case analysis with worst-case "current model" is done. The worst-case "cur-

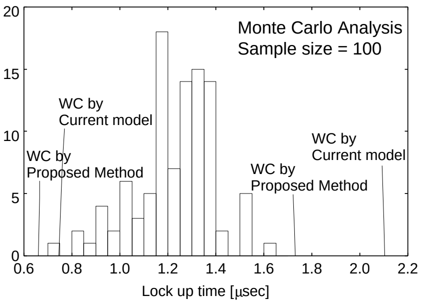

Fig. 11. Histogram of the PLL lock up time

TABLE I
Comparison of worst-case of lock up time (Unit [μsec])

Method of estimation	Best Case	Worst Case
Proposed Method	0.66	1.73
Current model	0.75	2.10

rent model" is defined as the worst-case parameters of the transistor current (Fig. 2), and it is often used as the worst-case of a circuit. In this worst-case analysis, R and C of the low pass filter are assumed to take their 3σ corners. The result of this corner analysis is also shown in Fig. 11 as "current model".

The comparison between the worst-case value by the "proposed method" and the "current model" is shown in Table I. From this, the worst-case values by the current model are not obviously real worst cases. Thus the accurate worst-case analysis needs a realistic method which takes account of the realistic statistical distribution of the physical parameters. Our proposed method can perform the realistic worst-case analysis with low simulation cost. From this, we can see the importance of the hierarchical statistical analysis.

The final application of the hierarchical statistical analysis is a sensitivity analysis. In order to examine the influence of each process-level variation to the lock up time behavior, the sensitivity of the lock up time against each non-correlated variables is calculated. Three non-correlated parameters with large $\partial r/\partial x_i$ are chosen, and the result which expanded them using Eq. (5) is shown in Table II.

From this table, we can see that L_d of NMOS is a dominant factor, and W_d and K_p of NMOS, L_d of PMOS as well, and physical explanation of this result can be given as follows. The lock up time depends on the capability of VCO oscillation frequency, and is consequently related with the transistor current characteristics.

The usual sensitive analysis is performed only in each layer, and it cannot reveal the effect of the physical parameter to system performance. Only above mentioned method enables us to link the statistical information, and to know the effect beyond the hierarchical layer. The reduction in those parameters could effectively reduce the variation in the PLL lock up time behavior.

TABLE II
Sensitivity of the lock up time (Unit [nsec])

NMOS

	L_d	W_d	K_p	N_ch	R_DS
x_1	**− 85.7**	−9.68	**−25.7**	8.98	−0.959
x_2	−2.38	**31.5**	8.01	−7.01	−0.953
x_3	−6.91	−10.6	4.78	−6.42	0.451

PMOS

	L_d	W_d	K_p	N_ch	R_DS
x_1	8.12	−0.895	5.14	−12.2	0.643
x_2	**29.9**	−0.436	2.16	15.5	2.3
x_3	**−25.2**	−0.997	−0.562	−7.71	1.69

IV. Conclusion

In this paper we presented a statistical analysis method which transfers the statistical information from process-level to system-level without loss. Using this method, we can not only perform the statistical analysis in system level, but also know the constraint on process parameter from system performance specification. This method was applied to a PLL for an experiment, and it was verified that proposed method enable to analyze the system level performance variability.

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