Embedded tutorial:

Issues on SOC Testing in DSM Era

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Deep sub-micron technology is rapidly leading to exceedingly complex, billion-transistor chips. By these technology evolutions, a system is integrated into a chip so called a system-on-a-chip (SOC). In order to bridge the productivity gap between available transistors and able to be designed in SOC, higher-level behavioral language and re-use of already designed intellectual property (IP) will become more common. However, these techniques affect test methodologies and failure analysis of SOC.

On the other hand, SOCs are implemented as a collection of heterogeneous circuits such like ASICs, DRAMs and analog circuits, so it will be large impact for Design for Testability techniques (DFT) and test cost issues. New test methods involving built-in-self-test (BIST) are required that will allow low-speed, low-cost Automatic Test Equipment (ATE) to test the digital portions of SOCs at high speed.

In the aspect of test quality, new fault models will be required to handle crosstalk and new failure modes that will result from multi-level metal structures. The old “stuck-at” single fault model is becoming less effective for computing expected test results for complex SOC.

This tutorial is based on the discussion in Test working group of Semiconductor Technology Roadmap Committee of Japan.