Design For Manufacturability:

A Path From System Level To High Yielding Chips

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Abstract - This tutorial describes a wide spectrum of the Design for Manufacturability (DFM) activities. We start by presenting a new approach to IC design, which takes full advantage of leading edge technology. Then we propose a new methodology for acceleration of yield ramping which accounts for all the dominant yield loss mechanisms and a set of software tools that have been developed to address the yield learning problems. Several real-life examples demonstrate the practical results of employing such a yield ramping strategy.

SUMMARY

Over the years, the increase in IC functionality has been achieved by a continuous drive towards smaller feature sizes. Due to the decreasing dimensions of semiconductor structures, the sensitivity to critical design and manufacturing parameters has risen dramatically. Vertical integration techniques and multi-level interconnect, which are becoming more common in modern technologies, have driven up the number of critical processing steps to several hundreds. These trends are expected to continue for the next several decades. The .13 micron technology is around the corner as well as 300 mm wafers. The increase in IC functionality has come with a skyrocketing capital spending (more than $2 billion per fabrication facility). Moreover, the product life cycles for leading edge IC's have become very short (less than 2 years).

In this age of multi-billion dollar IC fablines and increased time-to-market pressures, achieving profitable production in the shortest possible time becomes an absolutely necessary condition for survival. Increasing the initial yield and the rate of the yield ramp has the biggest impact on the profitability of the product since the price of the product in the market place will gradually decrease. Thus, the Design for Manufacturability (DFM) has become a really hot research topic.

This tutorial will cover the key aspects of the DFM activities. We will start by describing a new approach to IC design that can take full advantage of the capabilities of the state-of-the-art technology. This is a new paradigm, quite different from the technology-independent design methodology advocated several years ago. Critical design decisions must be made very early at the high levels of the design (e.g., choice of technology, design style, numbers of interconnect levels).

These decisions can be made only if the technology is properly characterized and the information is abstracted to higher levels to be useful to IC designers. We will present a design-manufacturing interface that is aimed at capturing statistical characterization of the IC manufacturing process. On the circuit level, this interface provides accurate prediction of the correlated sets of SPICE-level device parameters. On the layout level, the set of design rules is derived which allows for maximization of good chips per wafer. These rules

take into account not only the geometrical but also the electrical effects (such as coupling capacitances). Given such an interface, we will then describe methods for IC design optimization to provide the best matching between the IC performance and manufacturing process capabilities.

The second part of the tutorial will be devoted to the yield learning strategies. We will present a new approach to the acceleration of yield ramping which takes into account all the dominant yield loss mechanisms: parametric, systematic and random defect related problems. We will present several examples from the actual IC fabrication processes and demonstrate contributions of different components to the yield loss during the ramping stage. These will include contamination, design margins (process-design mismatch), process variations (e.g., critical dimension variations due to lithography and etching, interlayer dielectric thickness variations due to Chemical Mechanical Polishing) and lithographic errors (printability problems).

Finally, we will present a set of software tools that have been developed to address the yield learning problems. These tools can be divided into three categories: design analysis (e.g., defect-limited yield prediction based on critical area analysis), yield data analysis from all measurements available in the IC fabrication process (in-line, E-test, probe test) and yield diagnosis/design modification (circuit, layout and even process recipe). We will provide several real-life examples that will demonstrate the practical results of employing such a yield ramping strategy.