Hysteresis Effect in Floating-Body Partially-Depleted SOI CMOS Domino Circuits

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ABSTRACT

This paper investigates the basic mechanisms of hysteretic delay and noise margin variations for floating-body Partially-Depleted SOI CMOS domino circuits in detail. Three cases, based on whether the input signals are "domino input signals" from other domino circuits; "static input signals" from static circuits or latches; or a combination of "domino and static input signals" are examined and differentiated. It is shown that hysteretic delay variation is larger and noise margin worse for the later case with "mixed domino and static input signals." Although the delay and noise margin disparities between the three types of input signals are significant at beginning of the clock cycles, they converge as the circuit approaches steady-state.

1 INTRODUCTION

Silicon-on-insulator (SOI) technologies are maturing from research stage to commercial development for low-power and high- performance applications [1, 2, 3, 4, 5]. For high-performance applications, partially-depleted SOI (PD/SOI) devices are more favorable due to the better scalability and manufacturability by decoupling the threshold voltage from the silicon film thickness [3]. It is well known that the floating-body in the partially-depleted device causes hysteretic V_T and delay variations due to the long time constants associated with various body charging/discharging mechanisms resulting from the slow generation/recombination processes of excess carriers in the body region [6, 7, 8]. Experimentally, hysteresis has been shown to cause pulses to stretch or shrink as they propagate down a inverter chain [6, 7]. The hysteretic variation in V_T also affects the noise immunity of the circuit. It is crucial for circuit designers to quantify and contain the variations in both the circuit delay and noise margin to maintain and exploit the advantage of PD/SOI technology.

CMOS domino circuit is one of the most widely used circuit style for high-performance designs [9]. Although domino circuits are faster than their static counterparts, they are more susceptible to noise. The parasitic bipolar effect resulting from the floating-body in PD/SOI devices has been shown to reduce the noise margin and potentially cause logic state error if not properly accounted for [10]. Circuit techniques have been derived to overcome the parasitic bipolar effect and improve the noise immunity with minimal impact on the delays [5]. However, a detailed study of the hysteresis effect on domino circuits is still lacking. In this paper, we investigate the basic mechanisms of hysteretic delay and noise margin variations for PD/SOI CMOS domino circuits in detail. Three cases are examined and differentiated, based on whether the input signals are "domino input signals" from other domino circuits; "static input signals" from static circuits or latches; or a combination of "domino and static input signals." It is shown that the hysteretic delay variation is larger and noise margin worse for the later case with "mixed domino and static input signals." Although the delay and noise margin disparities between the three types of input signals are quite significant at beginning of the clock cycles, they converge as the circuit approaches steady-state.

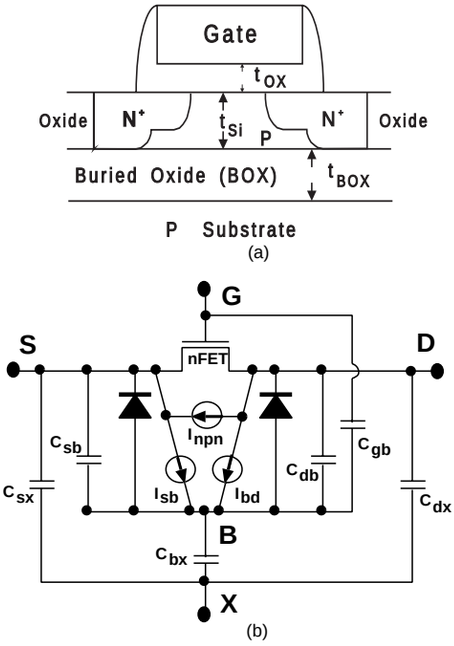


Figure 1: (a) Schematic cross-section of a PD/SOI nMOSFET, and (b) Equivalent circuit model (I_{npn} is the parasitic lateral NPN transistor collector current; the two diodes are the internal Emitter-Base and Collector-Base junction diode; I_{sb} and I_{bd} are the impact ionization currents.

2 DEVICE STRUCTURE AND CIRCUIT CONFIGURATION

The schematic cross-section of a PD/SOI nMOSFET is shown in Fig. 1(a). The device has a 0.12 μm effective channel length, 3.5 nm gate oxide, and silicon film thickness of 180 nm. The supply voltage is 1.8 V. Fig. 1(b) shows the equivalent circuit model of the PD/SOI nMOSFET [10]. The floating region under the MOS device channel acts as the base of the parasitic lateral bipolar device, with the base current supplied by impact ionization.

Fig. 2 shows the schematic of a 5-input OR domino circuit. A basic domino gate consists of a n-transistor logic structure whose output node DYN is precharged to V_{DD} by a precharge pMOS transistor, and conditionally discharged to ground by the evaluate nMOS transistors. In addition, the domino gate incorporates a static CMOS inverting buffer at its output. During the precharge phase, the clock is "Low" and node DYN is precharged to V_{DD}, and thus gate output Y is at "Low." In the evaluate phase, the clock goes "High." Depending on the state of the inputs, node DYN

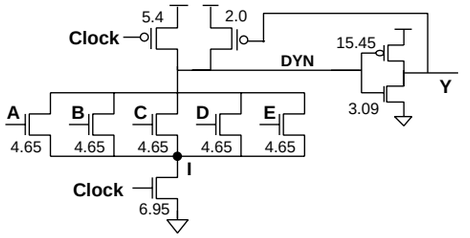


Figure 2: Schematic of a 5-input OR domino circuit.

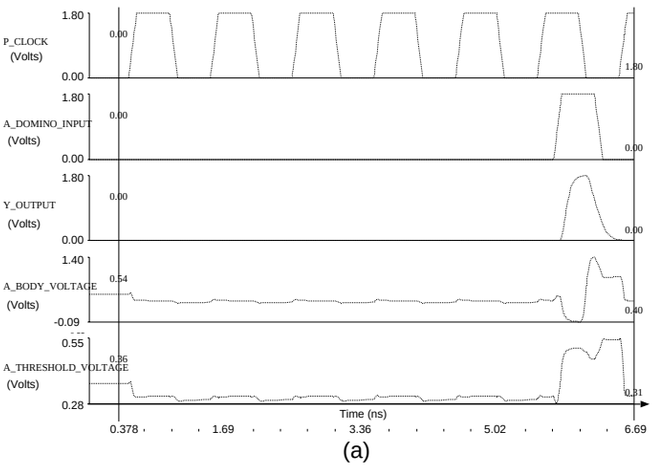
will either float at "High" level or will be pulled down. Correspondingly, the domino gate output Y will either remain "Low" or will get charged to "High." Thus, during the evaluate phase, the domino gate output Y can only make a transition from "Low" to "High." In a cascaded set of domino logic blocks, each stage evaluates and causes the next stage to evaluate. Any number of logic stages may be cascaded as long as the sequence can be evaluated within the evaluate clock phase.

Domino circuits can receive both domino and static input signals. As discussed before, the output of every domino gate falls (in the precharge phase) before the evaluate cycle and it conditionally rises during the evaluate cycle. In contrast, a unclocked signal, such as a static signal, does not follow the precharge and evaluate characteristics of a domino signal, i.e., it does not reset and conditionally rise in every clock cycle. Thus, the rise and fall transitions of a static signal can arrive at any time during the clock cycle (either during precharge cycle or evaluate cycle), and may erroneously discharge the dynamic node causing an incorrect evaluation of the domino gate. For the domino gate to evaluate correctly, the fall transition of a static signal must occur and settle before the onset of the domino evaluate cycle [11].

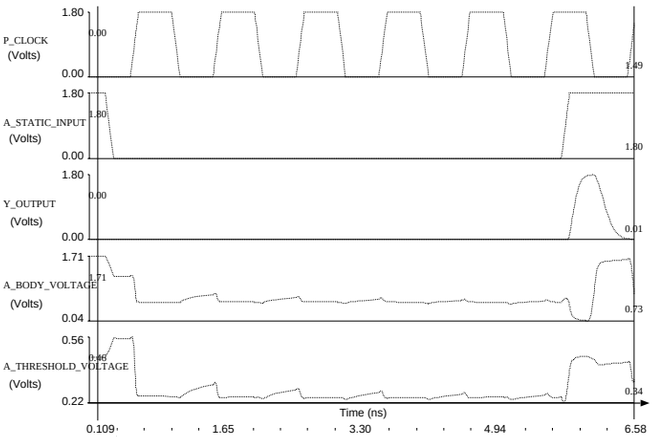
Fig. 3 depicts waveforms of clock, input A, and output Y for a 5-input OR gate (Fig. 2) for the cases where: input A is a "domino signal" (Fig. 3(a)); input A is a "static signal"(Fig. 3(b)); and input A is a "domino signal" while input B is a "static signal" (Fig. 3(c)), respectively. Also shown are the body voltages and the threshold voltages of the nMOS driven by input A through the clock cycles.

For the case of "domino input signal" (Fig. 3(a)), the clock is initially "Low" and the domino input A remains "Low" for a sustained period of time. The clock signal becomes active, corresponding to the situation when the circuit first starts operation either during chip start-up or when a gated clock domain is activated. The domino input signal A remains "Low" until it becomes active (rises to "High") during the 6-th evaluate clock phase, pulling down the dynamic node "DYN" and causing the output Y to rise. Subsequently, clock goes "Low" (i.e., precharge phase) and both A and Y are precharged "Low." Input signals B, C, D, and E remain "Low" all along. Initially, in the sustained precharge phase, the clocked evaluate nMOS is "off" and the switching nMOS-A (driven by the input A) has its drain precharged to V_{DD}. The body voltage of nMOS-A is determined by the balance of the reverse-leakage of its drain-to-body junction and the forward-current through the body-to-source junction (which flows as the leakage current through the "off" clocked evaluate nMOS). This initial body voltage can be seen to be 0.54 V in Fig. 3(a). Both the clock and signal have rise and fall time of 100 ps.

For the "static input signal" (Fig. 3(b)), the clock is "Low" while the static input A remains "High" for a sustained period of time. The static signal A falls before the first clock evaluate phase, and remains "Low" until it becomes active (rises to "High") during the 6-th evaluate clock phase. Except for the initial condition for A, the rest are identical to the previous case. Initially, with A at "High" and the clocked evaluate nMOS "off", the source of nMOS-A sits at one V_T below its gate voltage (i.e. V_{DD} - V_T. Notice that this V_T



(a)



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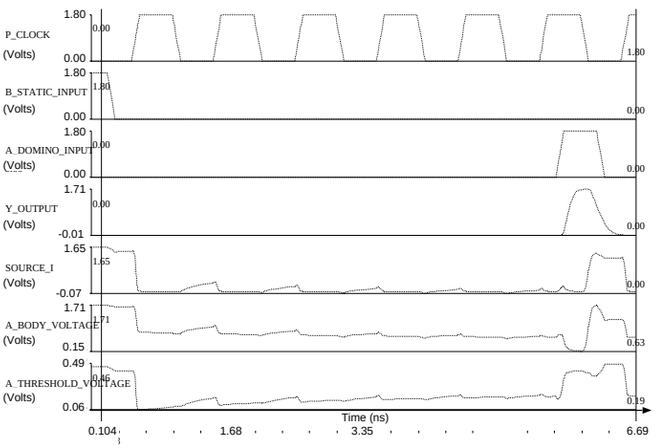


(c)

Figure 3: Waveforms for clock, input signal A, output Y, body voltage, and V_T for the 5-input domino OR gate for the case when : (a) A is domino input signal, (b) A is static input signal, and (c) A is domino input signal and B is static input signal (mixed domino and static input signals).

is lower than the regular V_T because of the positive body-to-source bias). The body of nMOS-A sits between its drain (precharged to V_{DD}) and source, and is very close to V_{DD} (1.71 V in Fig. 3(b)). When the input A falls before the first clock evaluate phase, the body voltage of nMOS-A is capacitively coupled down by the gate-to-body capacitance to 1.20 V as shown in Fig. 3(b). The source of nMOS-A is capacitively coupled down only slightly by the small gate-to-source capacitance, and remains considerably higher than the source voltage in the "domino input signal" case before the first clock evaluate phase.

In the case that the 5-input OR gate receives both "domino and static input signals" (Fig. 3(c)), the clock is initially "Low" and the domino input A remains "Low" while the static signal B remains "High" for a sustained period of time. The static signal B falls before the first clock evaluate phase, and remains "Low" thereafter. Domino input signal A remains "Low" until it becomes active (rises to "High") during the 6-th evaluate clock phase, pulling down the dynamic node "DYN" and causing the output Y to rise. Input signals C, D, and E remain "Low" all along. Initially, with B at "High" and the clocked evaluate nMOS "off", the source of nMOS-B (i.e., node I in Fig. 2) sits at one V_T below its gate voltage (i.e., V_{DD} - V_T=1.65 V. Notice that this V_T is lower than the regular V_T because of the positive body-to-source bias). The bodies of nMOS-A and nMOS-B sit between their drain node DYN (precharged to V_{DD}) and source node I, and are very close to V_{DD} (1.71 V in Fig. 3(c)). When the static input B falls before the first clock evaluate phase, the source of nMOS-B (node I) is capacitively coupled down by the gate-to-source capacitance (from 1.65 V to 1.47 V in Fig. 3(c)). The drop in voltage of node I capacitively couples down the body of nMOS-A slightly through source-to-body capacitance (from 1.71 V to 1.65 V in Figure 3(c)). This initial body voltage of 1.65 V is significantly higher than the body voltage for the pure "static input signal" case (1.20 V in Figure 3(b)) due to smaller coupling between source-to-body for the case in Fig. 3(c) as compared with the larger gate-to-body coupling for the case in Fig. 3(b).

In the following section, we discuss the basic mechanisms of hysteretic delay and noise margin variations for the three cases in detail.

3 RESULTS AND DISCUSSION

When the first evaluate clock pulse rises, the source node of nMOS-A is pulled down to ground by the clocked evaluate nMOS. The body of nMOS-A loses charges via the forward-biased body-to-source junction. The body voltage of nMOS-A is capacitively coupled down by the body-to-source capacitances (to 0.40 V for the "domino input signal" case in Fig. 3(a); to 0.52 V for the "static input signal" case in Fig. 3(b); and to 0.80 V for the "mixed domino and static input signals" case in Fig. 3(c)). Notice that the nMOS-A body voltage is highest (and thus V_T lowest) for the "mixed domino and static input signals" case When the evaluate clock pulse falls, the clocked evaluate nMOS turns "off", the dynamic node "DYN" is precharged to V_{DD}. The body of nMOS-A is first capacitively coupled up by its drain (the "DYN" node), and then slowly charged up by the off-state impact ionization current and the reverse-leakage through the drain-to-body junction.

Through the clock cycles, the body gains charges via impact ionization current and the reverse-biased drain-to-body junction current, and loses charges via the forward-biased body-to-source junction current. The net gain/loss of charges builds up from cycle to cycle, causing the body voltage to drift, until steady-state is reached. Hence, V_T and the circuit delay vary, depending on when (which clock cycle) the input signal A arrives. Fig. 4(a) shows the body voltage, V_T, and the circuit delay as functions of the number of clock cycles after which the input signal A rises for a 1.0 GHz clock. The corresponding cases for the "static input signals" and

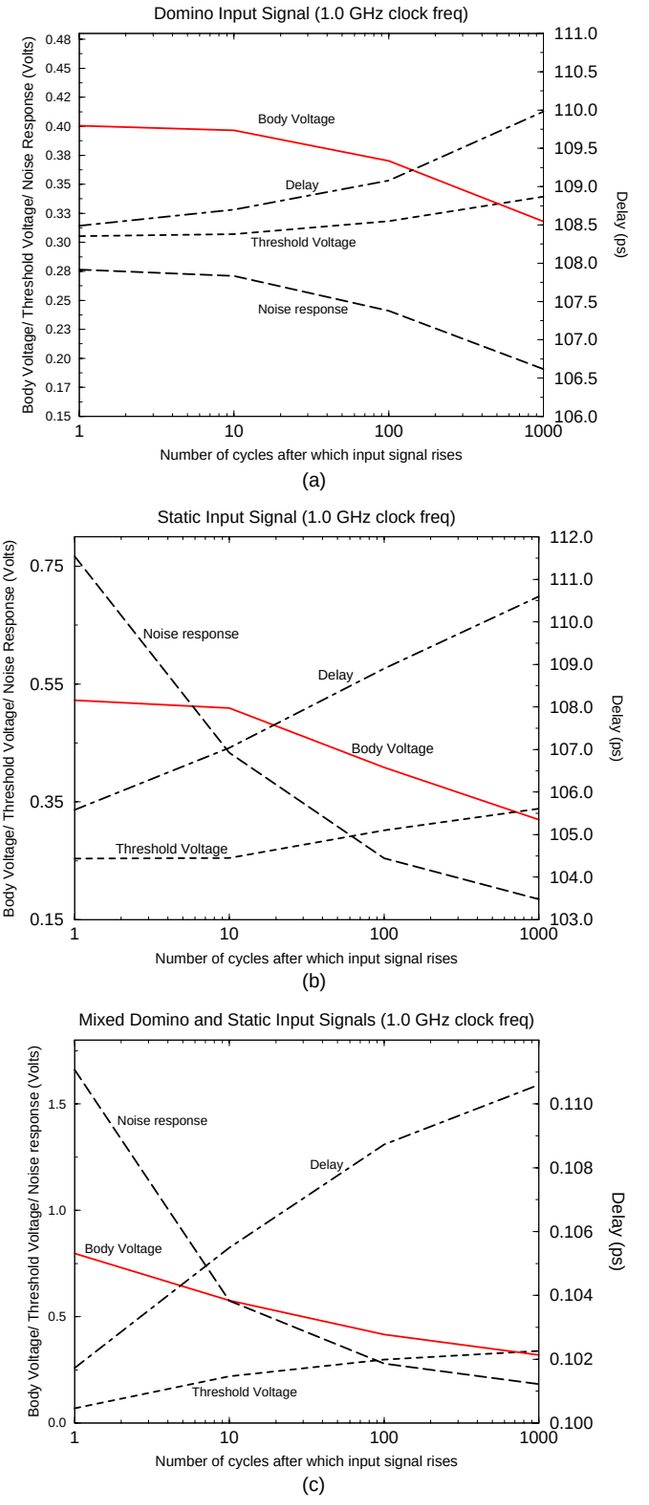


Figure 4: Variation in body voltage, threshold voltage, delay, and noise response with time (i.e., w.r.t. number of clock cycles after which input signal rises) for : (a) "domino input signal", (b) "static input signal", and (c) "mixed domino and static input signals."

"mixed domino and static input signals" are shown in Fig. 4(b) and Fig. 4(c), respectively. Notice that for the present configuration, nMOS-A loses body charges through the clock cycles, causing its body voltage to decrease, thus resulting in higher V_T and larger delay. The delay variation for the "domino input signal" is not significant (from 108.6 ps at first clock cycle to 110.0 ps at the 1000-th clock cycle, a variation of 1.29%) as can be seen in Fig. 4(a). For the "static input signal", due to the higher initial body voltage for nMOS-A as discussed earlier, the delay variation is more significant (from 105.6 ps at the first clock cycle to 110.6 ps at the 1000-th clock cycle, a variation of 4.73%). In the case of "mixed domino and static input signals", the delay variation is the most significant (from 101.4 ps at the first clock cycle to 110.6 ps at the 1000-th clock cycle, a variation of 9.07%) due to the highest initial body voltage for nMOS-A (as discussed in previous section).

As V_T increases through the clock cycles, the noise immunity of the circuit improves. Fig. 4(a) also shows the amplitude of the noise response as function of the number of clock cycles after which the noise inputs are applied. The input noise pulse has a 50 ps rise time, 25 ps plateau, 210 ps fall time, and amplitude of 0.7 V. All inputs receive the input noise pulse simultaneously, representing the possible worst case due to coupling noise. The amplitude of the noise response can be seen to decrease from 0.28 V at the first clock cycle to 0.19 V at the 1000-th cycle in the case of "domino input signal." The corresponding case for the "static input signal" is shown in Fig. 4(b) where the noise response is significantly higher at the beginning of the clock cycles (0.76 V at the first clock cycle). The noise response decreases to 0.19 V at the 1000-th clock cycle (same value as for the "domino input" case) as the circuit approaches steady-state. For the "mixed domino and static input signals" case, the noise response is highest at the beginning of the clock cycles (1.66 V at the first clock cycle) and it decreases to 0.19 V at the 1000-th clock cycle (same value as for the other two cases).

Fig. 5(a), Fig. 5(b), and Fig. 5(c) show the variations of the body voltages and delays through clock cycles with the clock frequency as a parameter for the three cases. Notice that the time constant associated with the body charging/ discharging for the nMOS is in the μs range, so it would take about $\approx 1\mu s$ for the circuit to reach steady-state. With decreasing clock frequency, the number of cycles to reach steady-state is decreased. Thus, in the case of 125 MHz clock, the body voltage and delay reach steady-state at $\approx$ 100 cycles as compared with $\approx$ 1000 cycles for a 1.0 GHz clock. Also notice that the body voltages and delays for different clock frequencies converge as the circuit approaches steady-state. This is because we are maintaining a constant 50% duty cycle, and the ratio of charge lost in the evaluate phase to the charge gained in the precharge phase is roughly constant for different clock frequencies (if we neglect the small off-state impact ionization current).

Fig. 6(a), Fig. 6(b), and Fig. 6(c) plot the "net charge leaving the body" per clock cycle as functions of the number of clock cycles for different clock frequency for the "domino input" case, "static input" case, and "mixed domino and static input signals" case respectively. The "net charge leaving the body" is obtained by integrating the impact ionization current, the reverse drain-to-body junction leakage, and the forward body-to-source junction current over the clock cycle. As can be seen, at low clock frequency, more charges are lost per clock cycle. Furthermore, at the same clock frequency, charges lost per clock cycle are highest for "mixed domino and static inputs" case and lowest for "domino input" case due to the corresponding variation in the initial body voltage.

Notice that the steady-state is independent of the initial states of the circuit, since it is determined only by the net charges gained/lost through the clock cycle (and is reached when the net charges gained/ lost through the clock cycle equal to zero). This can be clearly seen in Fig. 7 where the body voltages and V_T for the "domino input"

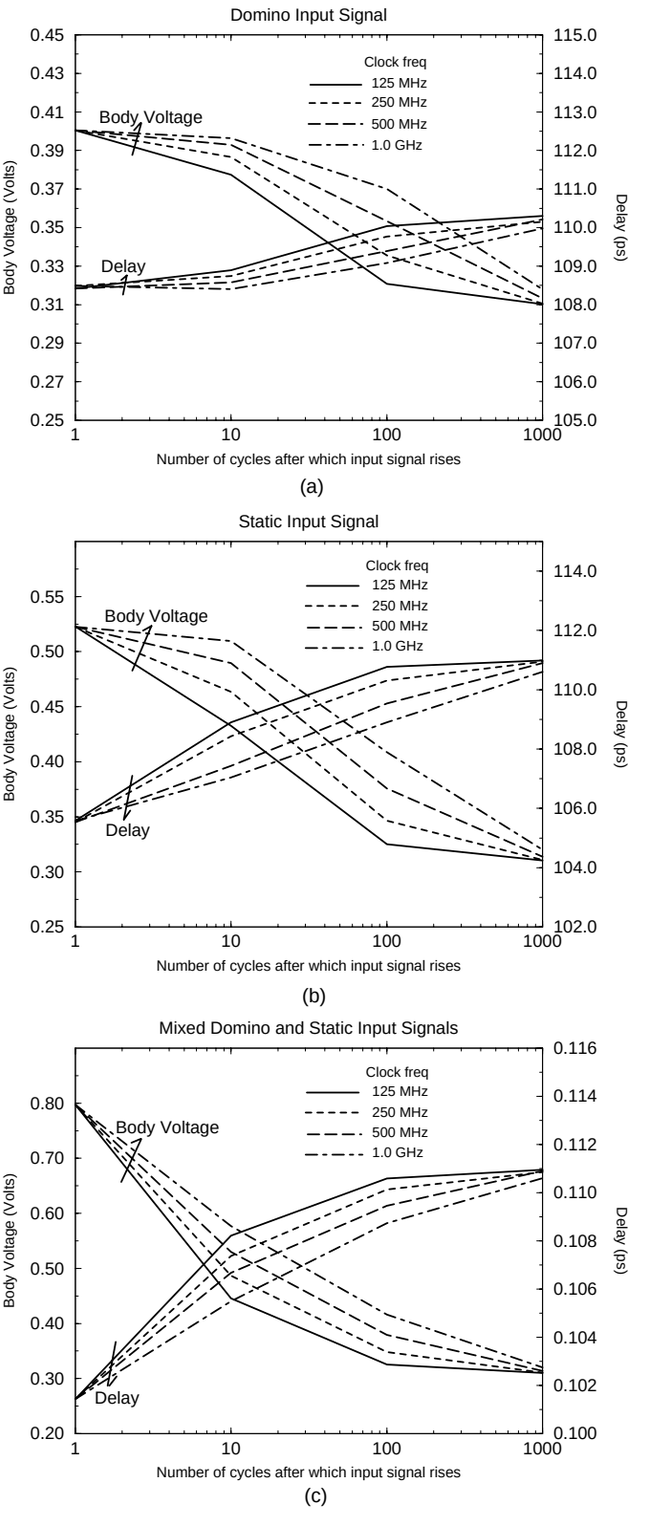
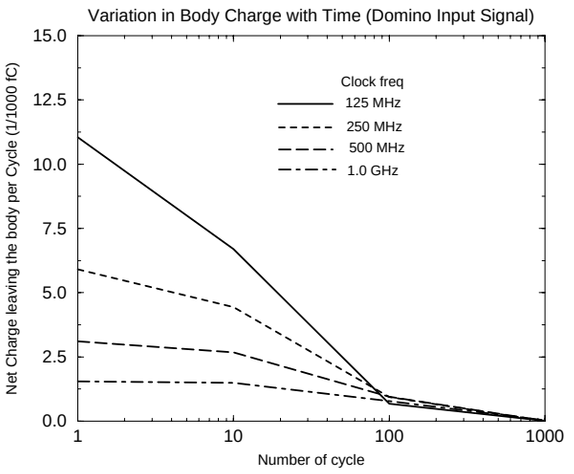


Figure 5: Variation of body voltage and delay with the clock frequency as a parameter for : (a) "domino input signal", (b) "static input signal", and (c) "mixed domino and static input signals."



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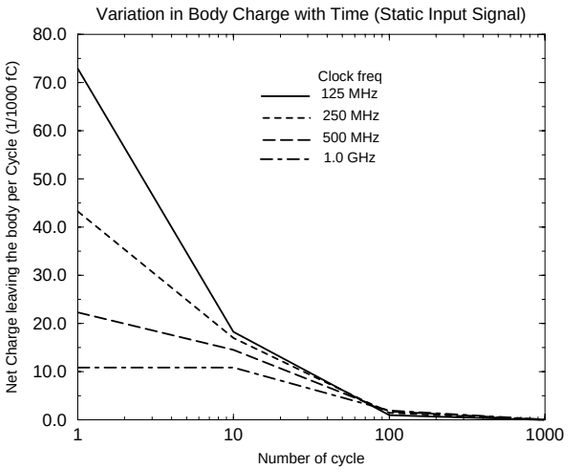

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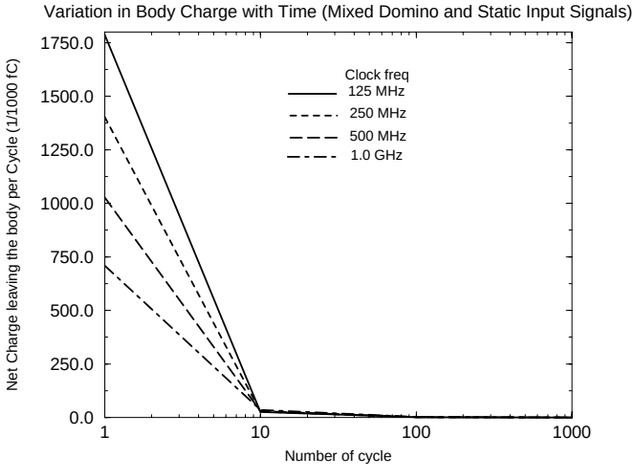


(c)

Figure 6: "Net charge leaving the body per cycle" as function of number of clock cycles with the clock frequency as parameter for the case of : (a) "domino input signal", (b) "static input signal", and (c) "mixed domino and static input signals."

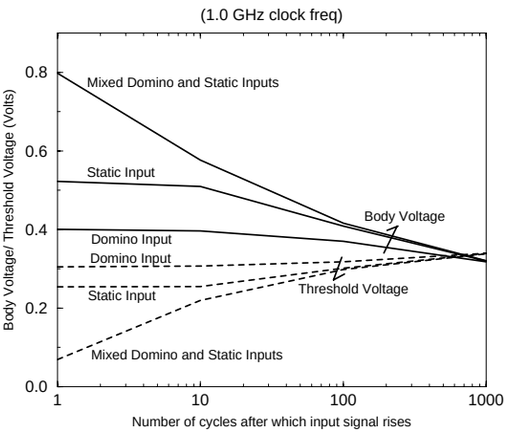


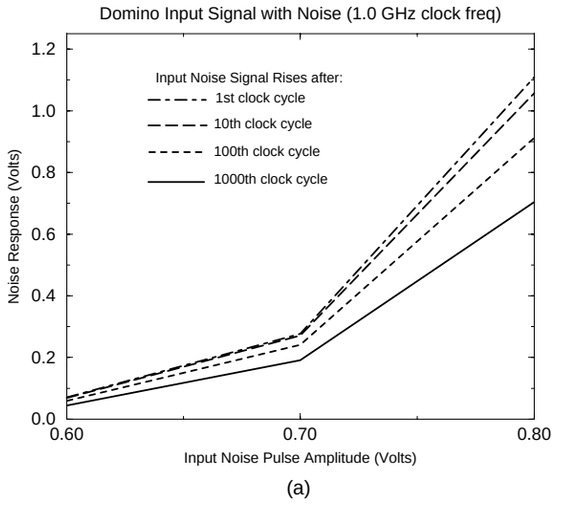
Figure 7: Convergence of body voltages and threshold voltages in steady-state for "domino input signal", "static input signal", and "mixed domino and static input signals."

case, "static input" case, and "mixed domino and static inputs" case converge as the circuit approaches steady-state.

Finally, Fig. 8(a) shows the amplitude of the noise response vs the input noise amplitude for "domino input" case with the number of clock cycles after which the noise pulse (50 ps rise time, 25 ps plateau, 210 ps fall time) is applied (simultaneously to all inputs) as a parameter. The circuit is most susceptible to noise when the clock first becomes active. As V_T increases through clock cycles, the amplitude of the noise response decreases. The corresponding case for "static input" case is shown in Fig. 8(b) where the noise response is significantly higher in the first clock cycle due to lower threshold voltage. As shown in Fig. 8(c), the circuit is most susceptible to noise in the case of "mixed domino and static inputs" where the noise response is the highest in the beginning due to the smallest V_T, but it converges with the noise response in the "domino inputs" case and "static inputs" case at steady-state (around 1000-th clock cycle).

4 CONCLUSION

A thorough understanding of the circuit behavior in a new technology is crucial in realizing its potential benefits. In this paper, we presented a detailed analysis of the basic mechanisms of hysteretic delay and noise margin variations for CMOS domino circuits in floating-body partially-depleted SOI technology. It was shown that when a domino circuit received its inputs from static circuits or latches, the hysteretic delay variation was larger and noise margin worse, compared with the case when the circuit received its inputs from other domino circuits. The hysteretic delay variation was the largest, and noise margin the worst, when the circuit received "mixed domino and static signals." The effect was attributed to the different initial body voltages of the switching logic transistor with different type of input signals. Although different types of input signals caused significant delay and noise margin disparities at the beginning of the clock cycles, they converged as the circuit approached steady-state. This study provided a basic understanding for circuit designers to better quantify and contain the hysteretic delay and noise margin variations which is crucial for fully exploiting the performance leverage of a scaled PD/SOI technology.



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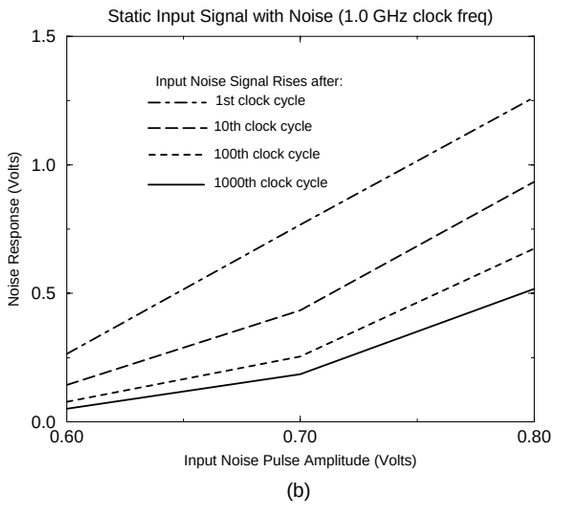

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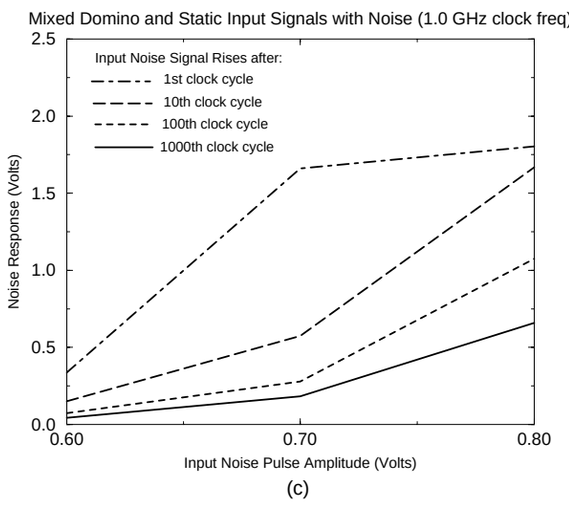

(c)

Figure 8: Amplitude of noise response vs input noise pulse amplitude with the number of clock cycles as a parameter for : (a) “domino input signal”, (b) “static input signal”, and (c) “mixed domino and static input signals.”

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