A Second-Order Sigma-Delta Modulator with Built-in VGA to Improve SNR and Harmonic Distortion

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Abstract

A modified architecture of the second-order switched-capacitor modulator is proposed. A simple four-transistor variable gain attenuator is included in the architecture which continuously adjusts the reference voltage of the quantizer feedback. This improves the output SNR for small signal input and reduces the harmonic distortion for large signal input. Simulation results show that it achieves higher dynamic range and lower harmonic distortions compared with the traditional architecture.

1. Introduction

The oversampling sigma-delta modulator A/D converters are widely used for signal acquisition systems in voice-band communications, digital audio, ISDN and other applications since they can provide high-resolution, high-linearity analog-to-digital conversion without accurately matched analog components [1]. Second-order sigma-delta modulators are quite tolerant of operational amplifier gain errors and relatively insensitive to integrator leakage resulting from finite DC gain in operational amplifiers as well as to offset voltages and comparator hysteresis [2]. Furthermore it has no complex stability problems which haunt higher order modulators. However, a problem with a second-order modulator that uses a single-bit quantizer, is that of overloading. The overloading occurs for AC input whose signal level is within approximately the top 10dB of the dynamic range. This produces harmonic distortion components for sinusoidal inputs, as well as significant tone components near fs/2 [3]. For the lowpass sigma-delta modulators, these harmonic distortions of lower frequency components contribute to large inband noise, which ultimately limits SNDR performance of the modulator. Since the quantization noise power is a constant if the modulator's order and oversampling ratio are fixed, the output SNR of the oversampling sigma-delta modulators decreases when the input signal signal decreases. This actually limits the dynamic range of sigma-delta modulators when very small signals are to be converted. The traditional method to improve SNR for the small signal input and reduce harmonic distortion for the large signal input is to add an AGC stage before the A/D converter. This will introduce more power consumption and extra chip area needed of the high dynamic range variable gain amplifier of the AGC. However, if we consider the ideal performance equation (1) of a sigma-delta modulator [8],

$$DR = \frac{3}{2}K^2\frac{2L+1}{\pi^{2L}}M^{2L+1} \qquad (1)$$

where DR is the dynamic range, L is the order of the modulator, M is the oversampling ratio and K is the ratio between the input signal amplitude and the reference voltage, we find that the dynamic range is proportional to K^2. This can be used to improve the small signal performance of the modulator.

A sigma-delta modulator A/D Converter with built-in variable gain stage is reported in [4]. It takes the advantage of the gain-control characteristic of the sigma-delta modulator. Instead of using an analog amplifier in front of the A/D converter, the reference voltage of the modulator is digitally adjusted by a 6-bit resistor network to achieve the same result. In this paper, a much simpler circuit of a fully-differential four-transistor variable attenuator is used to attenuate the reference voltage continuously. The chip area can be greatly reduced compared with the resistor network. Section II briefly describes the architecture and analyzes the SNR adjustment by the feedback reference level in second-order switched-capacitor sigma-delta modulator. In section III, the design of the building blocks is discussed

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and specifically the functionality of the four-transistor attenuator is presented in details. In section IV, simulation results of a traditional modulator and the new architecture are compared.

2. Sigma-Delta Modulator Architecture

Figure 1 shows the block diagram of the second-order sigma-delta modulator with the internal AGC loop. In this

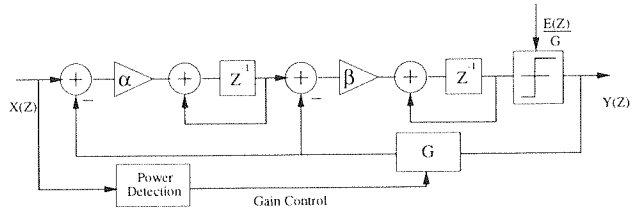

Figure 1. Second-order Switched-Capacitor Sigma-Delta Modulator Discrete Time Model

architecture, the adjustable amplification is realized by the variable attenuation of the reference voltage and is set by the gain control signal whose amplitude is proportional to the input signal amplitude. The gain control comes from the differential output of the power detection circuit . Because the time constant of the AGC loop is much larger than the period of the input signal, the feedback effect of the internal AGC loop can be neglected when the sigma-delta modulator is analyzed. The equivalent discrete time model for the modulator is changed by adding an attenuation factor G, which attenuates the reference voltage by the factor G, between the quantizer output signal and the feedback to the two adders. Note that because of the change of the reference voltage, the average quantization noise E should also be scaled to E/G. With this model the output signal can be expressed as the summation of the input signal X and quantization noise E [4]:

$$Y(Z) = GX(Z) + (1 - Z^{-1})^2 E(Z) \qquad (2)$$

where we assume $\alpha = 1$ and $\beta = 1$ in Figure 1. Because oversampling ratio is far greater than 1, we can approximate $z = 1$ within the signal bandwidth in the above equation. The above equation shows that the signal $X(Z)$ is amplified by factor G while the noise remains the same. Then G can be seen as a gain factor for the signal. Ideally, this will increase the SNR by factor G^2. However, in the above analysis, the internal thermal noise, flicker noise and noises caused by nonideal circuit effects are not included. Because these noises are generated at the same node as that of the input signal, they have the same transfer function if they fall into the signal bandwidth. Thus the SNR improvement by reducing the reference voltage is only valid for quantization-noise-dominated sigma-delta modulators. In other word, the method can not be used for very high-resolution sigma-delta modulators, whose performance is mainly limited by the internal noise of the first integrator.

On the other hand, harmonic distortion components will be increased drastically when the ratio between the input signal and the reference voltage is greater than -10dB. Since G can be dynamically controlled according to the input signal power, harmonic distortion components are expected to be reduced by decreasing G which has the same effect of decreasing input signal amplitude.

3. Circuit Design

An experimental second-order modulator is implemented in 1.2 μm CMOS parameters and oversampling ratio of 64 is chosen to enable all the simulations be done with SPICE [7]. This will achieve more accurate results compared with other macromodel simulation tools. Note that because SPICE can not do transient analysis including thermal noise and flicker noise of the transistors, the simulation result is only valid for quantization noise dominated modulators.

The operational amplifier is the most important component in the design of the sigma-delta modulator. The operational amplifier used in switched-capacitor integrators theoretically need only to have open-loop gain equal to the oversampling ratio [2]. In practice, this gain needs to be significantly higher in order to suppress harmonics caused by op-amp nonlinearities [5]. The op-amp design used in this implementation is a differential folded-cascade PMOS input stage followed by an output stage as shown in Figure 2. Simulations show that the op-amp has a DC gain of 74dB, a phase margin of 84 degree with 200ns settling time.

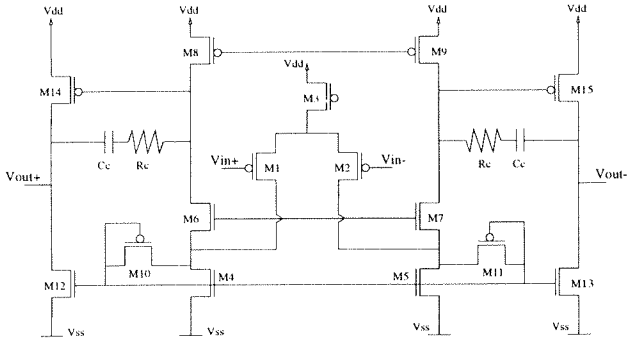

Figure 2. Operational Amplifier Schematic

The comparator-latch combination implements the single-bit quantizer. A high-speed comparator [6] in Figure 3 is designed with the sampling rate up to 80MHz and 8-b accuracy.

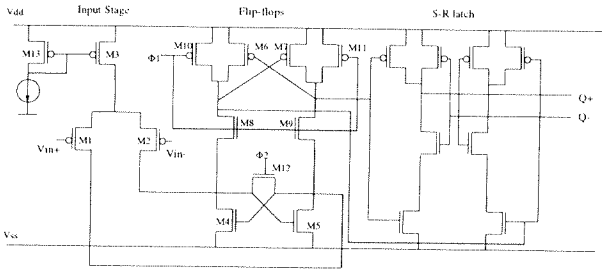

Figure 3. Comparator Schematic

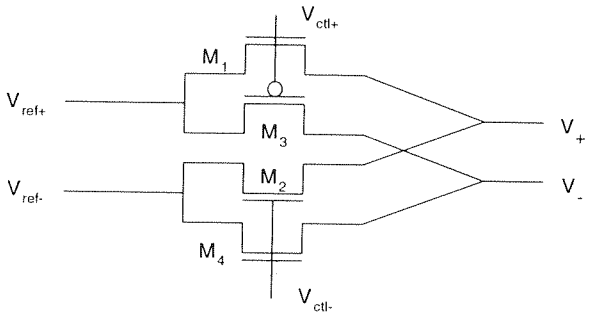

Figure 4. Four-transistor attenuator

The variable gain stage is realized by a four-transistor attenuator. Using two pairs of compensated transistors, the differential variable reference voltage is obtained. Assume that the transistors are operating in the saturation region. Apply two differential voltages at V_{ctl+} and V_{ctl-}, which are generated by the power detection circuit in the modulator. Let

$$V_{ctl+} = V_{cm} + \Delta \quad (3)$$

$$V_{ctl-} = V_{cm} - \Delta \quad (4)$$

where V_{cm} is the common voltage of the differential output of the power detection circuit and Δ is the differential part, which shows the amplitude of the input signal. Furthermore, let NMOS transistors M1, M2 have the same values of W and L and PMOS transistors M3, M4 have the same values of W and L. From the current equations:

$$I_{DS1} = I_{DS2} \quad (5)$$

$$I_{DS3} = I_{DS4} \quad (6)$$

we can obtain the linear relation:

$$V_+ = 2\Delta - V_{ref-} \quad (7)$$

$$V_- = V_{ref+} - 2\Delta \quad (8)$$

These equations show that output voltage is only determined by the differential control input and the reference voltage. They are not only independent of the value of V_{cm} but also insensitive to the threshold voltage.

4. Simulation Results

For the simulations, a 1.2μm CMOS technology and supply voltage of 3V have been used. Two second-order modulators have been simulated and the resulting SNR verses input amplitude curves are depicted in Figure 5. The control voltages are set so that the adjusted reference voltage is always three times larger than that of the input signal. For these simulations, a clock frequency of 50MHz, a 39KHz input signal is used. It shows that the SNR keeps almost the same level while the input signal is decreasing in the modified architecture. When the input signal is smaller than -40dBm, because of the resolution in SPICE, the simulated SNR drops. For the practical circuit, thermal noise and flicker noise will limit the SNR when the input signal is very small. Figure 6 and Figure 7 are the power spectra of the two modulators with the same input signal level. It clearly shows that the overloading effects are improved for the modulator with internal AGC.

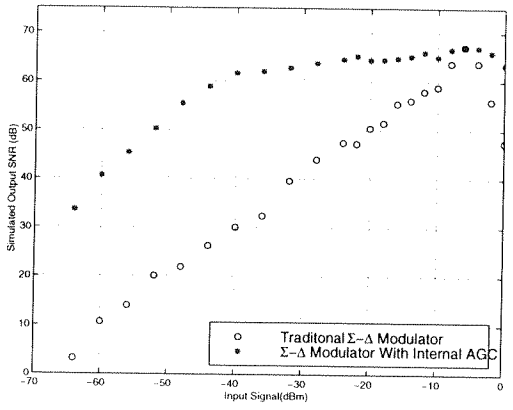

Figure 5. Output SNR Comparison

5. Conclusions

Adding a variable gain stage in the second-order sigma-delta modulator has several benefits to the whole ADC system. First the built-in variable gain stage has the same effect as an analog amplifier in front of the ADC converter so that the complexity of the previous AGC stage can be greatly reduced. Second this gain stage offers a voltage tuning parameter for the modulator which makes the nonlinear and stability problems easy to be dealt with. Device level simulations in this paper show the feasibility and advantages of this architecture.

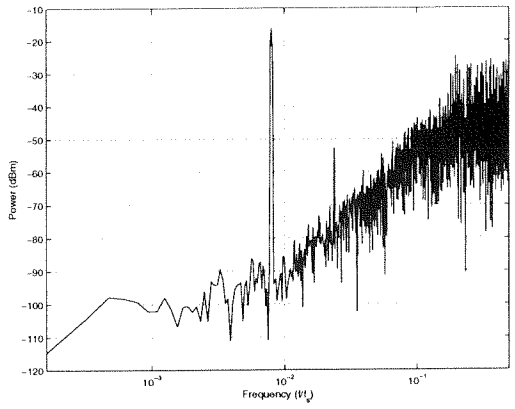

Figure 6. Modulator Output Power Spectrum Density without internal AGC

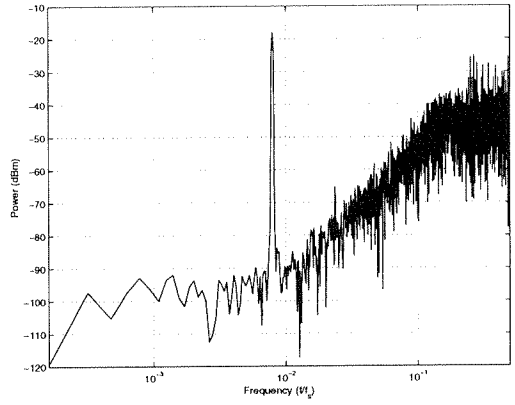

Figure 7. Modulator Output Power Spectrum Density with internal AGC

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