Low Power Chip Interface based on Bus Data Encoding with Adaptive Code-book Method

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Abstract

An adaptive code-book encoding is proposed, which is applicable for low power chip-interface. In this method, data transition activity on bus signals is lowered by data encoding similar to the vector quantization (VQ). Transferred data on bus are the quantized vector numbers along with the Hamming difference between the original data and the quantized vector. A computer simulation and measurement results show that this encoding method is effective for low power chip-interface especially for the deep sub-micron VLSIs.

1. Introduction

Recently the interest in VLSI design has shifted to minimizing the power dissipation from the conventional design criteria such as the minimum chip area and high speed operation. Especially, power reduction of chip interface circuits has become serious concern for low power VLSI design, as the power dissipation related to the chip interface is becoming the major part of the total chip power dissipation. From this point, several power reducing methods have been proposed[1, 2, 3]. They mainly however reduced power dissipation by reducing signal swing.

Alternative method for power reduction of chip interface was bus invert coding[4] which reduced power dissipation by inverting data so as to restrict signal transition at most to the half of the total bits in bus. This method was proposed for lowering peak power dissipation as well as average power dissipation, and the former leads to suppressing an undesired increase in simultaneous switching noise and metal electromigration.

Although the bus invert coding was proposed for the above mentioned purposes, we regarded it as a sort of the vector quantization (VQ)[5] method, where the quantized vectors are all-zeros and all-ones. In the bus inverting method, the quantized vector is transmitted using an additional signal line with the bus signals, that convey the Hamming distance from the quantized vector.

In this paper we propose a new power reduction method in chip interface circuits, which is generalization of the bus invert coding from the view point of the VQ. In section 2 we describe the encoding method which reduces signal transition. In section 3 we show computer simulation results of the present method. A test chip is shown in section 4 designed for evaluating merits and demerits in terms of power reduction and additional delay time.

2. Encoding and Decoding Method

Until now, two encoding methods which reduce signal transition on bus have been proposed; bus invert coding, generalized invert coding[6]. In the bus invert coding, the number of transition bits in data is counted, and when it is more than a half of the word length, the invert code is transferred with a flag signal indicating

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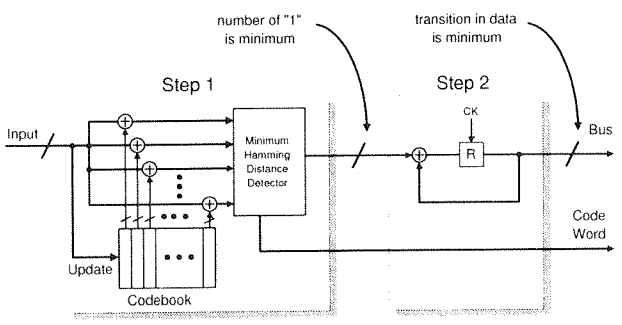

Figure 1. Data encoder based on the adaptive code-book encoding

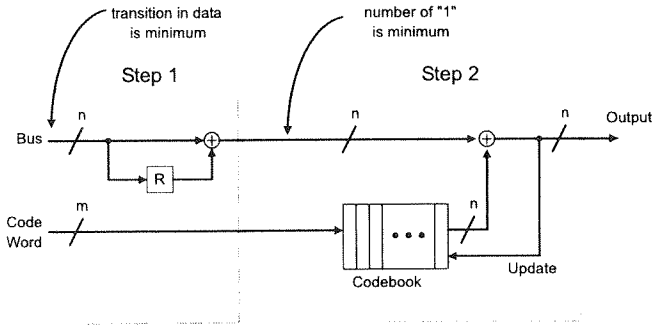

Figure 2. Data decoder based on the adaptive code-book encoding

the inversion. Otherwise the data is transferred as it is. In the generalized invert coding, a data word is compared with all the code data stored in a code-book to find the nearest code in the Hamming distance. Then the Hamming distance is transferred on the bus along with the selected code.

From a view point of VQ, this method is regarded as data compression, where the selected code is the quantized vector and the Hamming distance is the quantized error.

2.1 Encoding Method

An adaptive code-book encoding we propose in this study is developed based on the generalized invert coding (code-book encoding). Here the code-book is updated adaptively. Figure 1 shows a diagram of the adaptive code-book encoding scheme, which is summarized as follows,

1) The first step is a selection of a code in the code-book. Data words are successively compared one by one with the set of the codes to find the nearest codes in the Hamming distance. The output of the first step is a stream of the minimum Hamming distances, where numbers of "1"s are minimized.

2) The second step is a data transmission to the bus lines. Indexes of selected codes in the first step are successively set with Hamming distances difference data stream. Here the difference data stream is the Hamming distances encoded by the "non-return-to-zero (NRZ)" mode, so that transition of bus signals is minimized [1].

3) The third step is the code-book updating. By this updating the bus transition activity decreases much effectively compared with [4].

[1] Contrarily, for cases such as optical fiber links, this step is unnecessary.

2.2 Decoging Method

Data decoding is realized by bit-wise exclusive-OR operations of the codes, indicated by the code indexes, and bus data stream received in the previous cycle. Code-book in decoder is also updated just on the same way as the code-book in the encoder. Figure 2 shows a diagram of the adaptive code-book decoding scheme.

3. Evaluation by Simulation

We have evaluated effectiveness of this coding scheme using a logic level simulation, where the data word is 16-bit and the number of codes in the code-book is 16. We used two kinds of data for simulation.

3.1 Evaluation with Random Bus Data

Figure 3 shows simulation results of the total signal transitions in the difference data stream and the code indexes, normalized by the transitions in the conventional bus scheme, with "1"s weight in the input data as a parameter.

This indicates that the present method decreases the transitions most effectively, where "1"s weight in the input data is about 50%. And the reduction of the transitions is almost equivalent to the bus invert coding and the generalized invert coding for other conditions.

3.2 Evaluation with Data from a Personal Computer's Bus

Table 1 shows results of simulation using measured data from a personal computer's bus by a logic analyzer. It indicates that the present method reduces the signal transition in the actual situation most effectively.

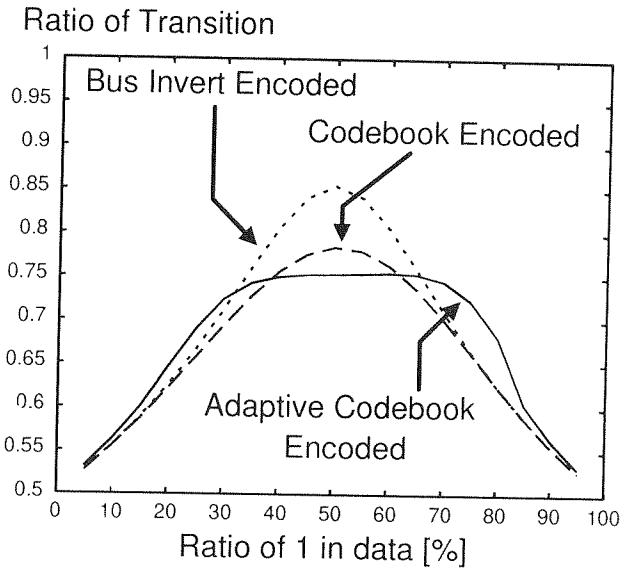

Figure 3. Comparison of signal transition decrease in several bus coding methods.

Table 1. Reduction of signal transition by each encoding method (Input data is extracted from PC's bus)

encoding method	signal transition			
	data	code word	sum	%
raw data	173587	0	173587	100%
bus invert	187996	4306	192302	110%
generalized bus invert	165596	14035	179631	103%
adaptive code-book	117055	14139	131194	76%

As described above, the adaptive code-book encoding reduces signal transitions most effectively for all types of data because of adaptable algorithm. Achieved reduction in the signal transition is about 25 – 50%. The worst case (about 25%) occurs on the condition that correlation in data stream is low, namely data stream is random. Higher correlation in data stream makes signal transitions lower.

4. A test chip

In order to evaluate the power reduction and an additional delay time in data encoding, we have designed a test chip using 0.5μm CMOS technology [2].

[2]The VLSI chip in this study has been fabricated in the chip fabrication program of VLSI Design and Education Center(VDEC), the University of Tokyo with the collaboration by NTT Electronics Corporation and Dai Nippon Printing Corporation.

Table 2. Chip specifications

Full custom 16-bit encoder/decoder	
Process	0.5μm CMOS 2-metal layer
Die size	4.8mm×4.8mm
Clock frequency	10MHz (at 3.3V)
Number of Tr.	50k
Package	120pins PGA[13×13] (I/O 76pins)

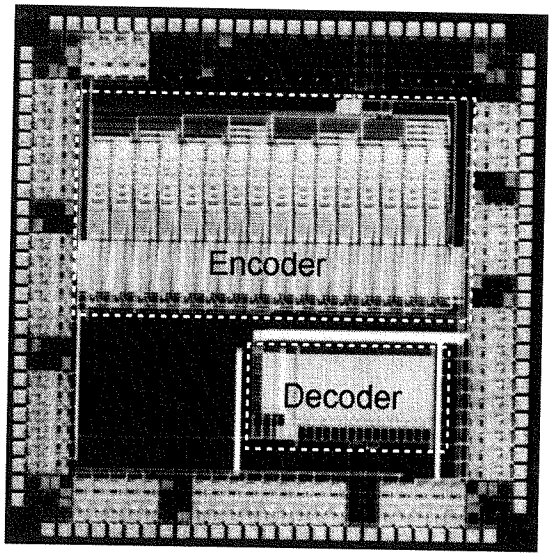

Figure 4. Chip micro-photo of the test chip for data encoder and decoder for low power chip interface

4.1 Chip Specifications

Table 2 shows specifications of the test chip and figure 4 shows a micro-photo of the test chip. The test chip consists of the encoder and the decoder. The minimum Hamming distance detector of encoder is realized by counters of "1"s, like compressors of Wallace-tree multiplier, and comparators. Data word is 16-bit just same as the simulation. The code-book size is variable(1, 2, 4, 8 and 16 codes).

4.2 Measurement Results

The delay time in the data encoding is 48[ns] for code-book size of 16 The power dissipation for encoding and decoding is 3.6[mW] at supply voltage 3.3[V] and the operating frequency 10[MHz]. On the other hand, power reduction in chip interface obtained by

Table 3. The minimum length where adaptive code-book encoding is effective (0.5um CMOS)

layer	wiring capacitance of unit length	minimum length
1-metal	200fF/mm	7.5cm
2-metal	150fF/mm	10cm
PCB	0.5pF/cm	30cm

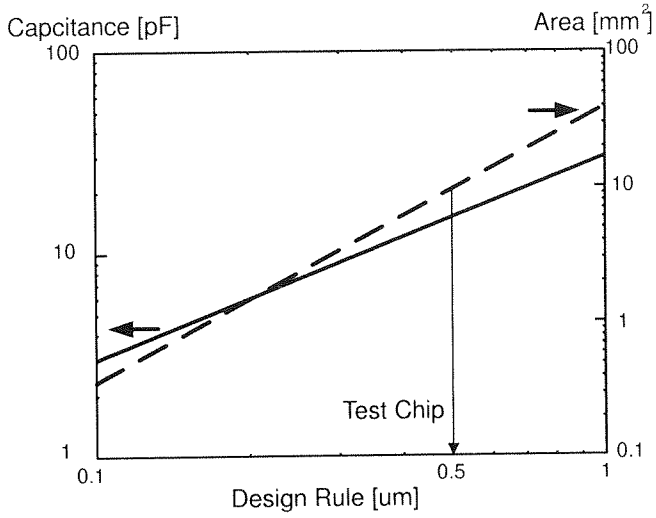

Figure 5. Power dissipation and chip size of encoding chip at each generation

the chip depends on capacitance on bus lines. So, the total power reduction is achieved for the bus capacitance more than 15[pF] for each signal line in this case(namely 0.5μm CMOS technology). Table 3 shows the minimum effective bus length in several situations. As the process feature size shrinks, the minimum effective length becomes shorter, so that this method becomes more effective in future. Figure 5 shows the power dissipation and the chip area of the encoder at each process generation. When design rule will shrink to 0.1μm, the minimum wiring capacitance will be less than 3[pF]. The area of the encoder will also become negligible small in the total chip area.

5. Conclusions

In this study we have described a new data encoding method for low power chip interface. The simulation results showed that this method decreases 25 – 50% signal transitions compared with the conventional non-coded data transfer. As this method is adaptive to data stream, it decreases signal transition for all sorts of data stream. We designed a test chip for encoding / decoding to evaluate the delay time and the power reduction. From measurement results, this method is effective for data transfer through large wiring capacitance such as bus lines. The chip size for encoding and decoding will become negligible as the design rule shrinks in near future. It also indicates that this encoding method will be effective for multi-CPU environments.

References

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