# THE DESIGN OF CMOS GIGAHERTZ-BAND CONTINUOUS-TIME ACTIVE LOWPASS FILTERS WITH Q-ENHANCEMENT CIRCUITS

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## ABSTRACT

A tunable second-order lowpass filter architecture capable of operating in the gigahertz frequency range is proposed. Two Q-enhancement techniques are utilized to extend the Q tuning range. Simulation results employing standard $0.5\mu m$ CMOS technology have successfully verified that the center frequency tuning and the hybrid Q-tuning approach operate between 1.26GHz and 2.3GHz center frequencies with Q larger than 1000. A tunable lowpass filter with a center frequency at 2.07GHz with a Q equal to 31 is designed to have 44dB input dynamic range and 27.8mW power dissipation.

## 1. INTRODUCTION

Recently radio frequency circuit implementation in submicron CMOS technology has received intense attention because it would allow integration of other digital signal processing circuits, providing a low cost single-chip solution [1][2]. In telecommunication applications, gigahertz-band filters with high quality factors (Q) are necessary, but are difficult to produce in a standard digital CMOS process.

Considerable research has been conducted for years to develop high performance monolithic filters for high frequency operations. A dominant high speed continuous-time filter implementation, called the OTA-C filter [3][4][5], uses an open-loop integrator as a basic building block, exploiting an operational transconductance amplifier whose high impedance output port is terminated with an integrating capacitor. However, attempts to reach higher operating frequencies have met difficulties due to excess phase problems [6]. Such filters with center frequencies ranging from a few kHz up to low hundred MHz have been reported [7]. Another approach is to exploit the high frequency attributes of transistors as filter elements to simulate passive filters [8][9].

This paper describes a second-order filter configuration based on the second approach for implementation of the lowpass functioning capable of operating in the gigahertz frequency range with a quality factor of interest. Emphases are placed on detailed design topologies including the transfer function and Q-enhancement techniques. Noise performance and linearity are also discussed.

## 2. LOWPASS FILTER CIRCUIT TOPOLOGY

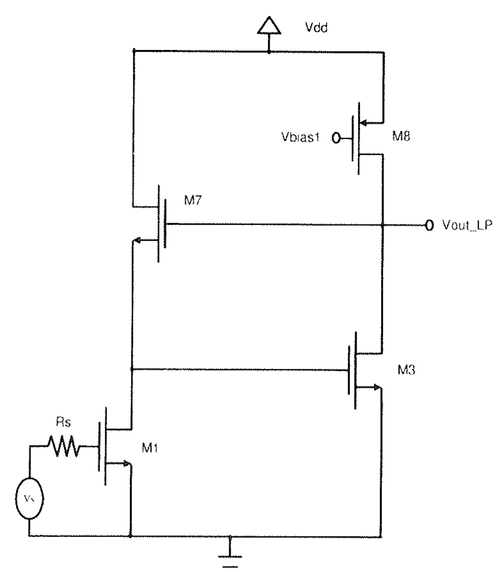


Figure 1: A basic lowpass filter schematic with a low quality factor.

The basic lowpass filter is illustrated in Figure 1. It can be proved through small signal analysis that the frequency response is a simple second-order transfer function with a pair of complex poles, which can be viewed as a lowpass filter. The shortcomings of this simple configuration are that the Q of the filter is quite low (usually less than 2) and strong dependence exists between the frequency and Q tuning. However, both problems can be solved by introducing extra Q-enhancement circuitry. Figure 2 shows a second-order lowpass filter schematic with Q-enhancement circuitry. In this figure, transistors M1 and M2 comprise the input amplifier cascode stage. This configuration offers several advantages that include reducing the Miller Effect at the gate terminal of the transistor M1, increasing the effective isolation between the input stage and the following stage, and improving the stability of the circuit. The core components of the filter are formed by transistors M3, M6, M7, and M8. This negative feedback configuration constrains the gate of the transistor M3 to a very low impedance node.

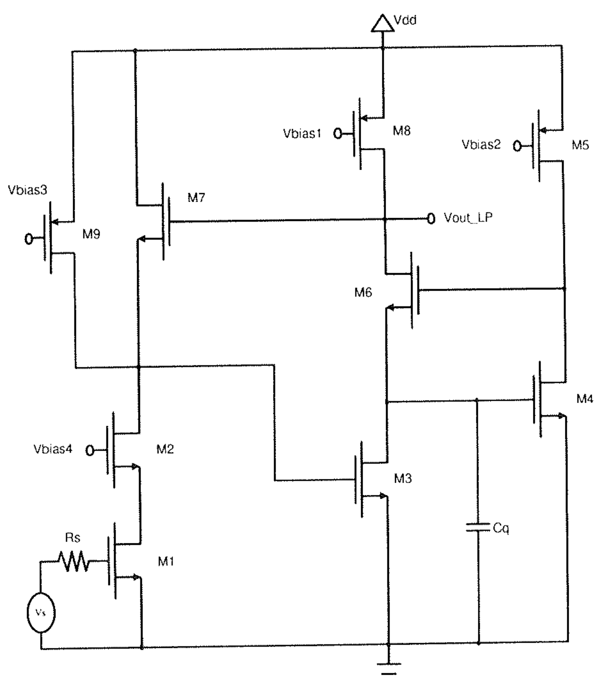


Figure 2: The second-order lowpass filter schematic with Q-enhancement circuitry.

Assuming $g_m >> g_{ds}$ for all transistors and ignoring all non-dominant high-order terms, it can be proved that the transfer function of the lowpass filter is approximately equal to

$$A_{v\_LP}(s) = \frac{V_{out\_LP}(s)}{v_s(s)}$$

$$\approx \frac{g_{m1}\, g_{m3}}{c} \frac{1}{s^2 + s\, A + B} \quad (1)$$

where

$$\begin{aligned} A &= \frac{g_{m6}\,(g_{m3}\, c_2 + g_{m7}\, c_3) - g_{m3}\, g_{m7}\, c_4}{g_{m6}\, c} \\ B &= \frac{g_{m3}\, g_{m7}}{c} \\ c &= c_1\, c_2 + c_2\, c_3 + c_1\, c_3 \\ c_1 &= c_{gd2} + c_{db2} + c_{gs3} + c_{gb3} + c_{sb7} + c_{gd9} + c_{db9} \\ c_2 &= c_{gs7} \\ c_3 &= c_{db6} + c_{gb7} + c_{gd7} + c_{db10} + c_{gd10} \\ c_4 &= c_{db3} + c_{gb4} + c_{gs4} + c_{sb6} + c_q \end{aligned}$$

$c_1, c_2$, and $c_3$ represent accumulated parasitic capacitance in the circuit, and $c_4$ represents an extra physical Q-enhancement poly-silicon capacitor $c_q$ in shunt with the parasitic capacitance of other transistors existing at the drain of the transistor M3.

By definition, the center frequency of the bandpass filter $\omega_o$ is given by

$$\omega_o = \sqrt{\frac{g_{m3}\, g_{m7}}{c}} \quad (2)$$

and the quality factor of the filter is therefore equal to

$$Q = \frac{g_{m6}\, \sqrt{c\, g_{m3}\, g_{m7}}}{g_{m6}\,(g_{m3}\, c_2 + g_{m7}\, c_3) - g_{m3}\, g_{m7}\, c_4} \quad (3)$$

Eq.2 reveals that the center frequency is determined by the transconductance of the transistors M3, M7, and $c$, the parasitic capacitive effect exhibited in the circuit. Here the transconductance of the transistor M7 is chosen as a prime candidate to be tuned by varying Vbias3 while Vbias1 and the input DC bias voltage of transistor M1 remain constant. An observation that can be made from Eq.3 is that the Q can be independently tuned by varying the capacitance $c_4$ without altering the center frequency $\omega_o$. Simulation shows that by properly sizing all transistors to achieve center frequencies at 1GHz and 2.2GHz with Q over 500 requires an extra capacitor $c_q$ equal to 0.9pF and 0.2pF, respectively.

Further insight can be gained by considering the other high frequency parasitic poles and zeros implicitly presented in the circuit, but not shown in Eq.1 due to analytical complexities. However, assuming the core feedback loop is broken, increasing the values of the capacitor $c_q$ and Vbias2 generate more phase shift at the output unity-gain frequency since the parasitic poles and/or zeros tend to move to lower frequencies, thereby decreasing the phase margin of the open-loop

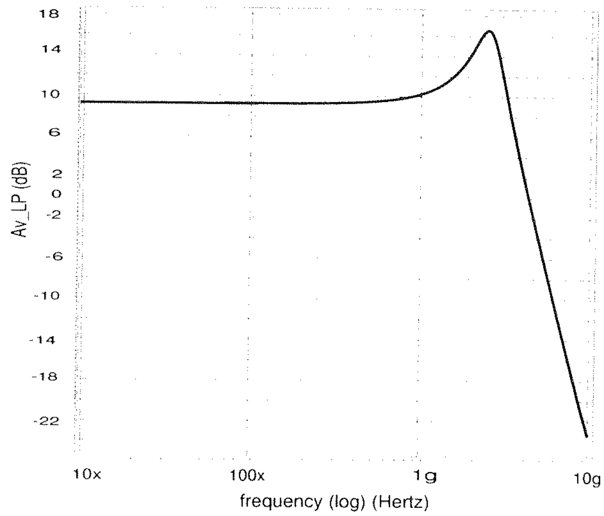


Figure 3: The lowpass filter frequency response with $f_o$=2.48GHz and Q=2.4 (without $c_q$).

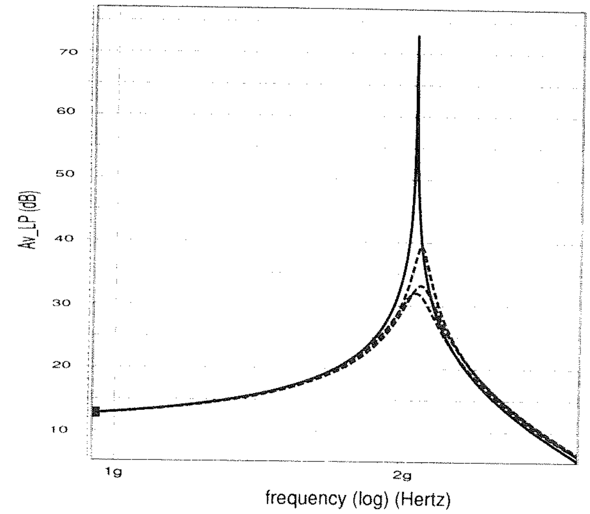


Figure 4: The independent Q tuning of the high-Q filter with a center frequency at 2.07GHz (with $c_q$=0.35pF).

circuit and boosting the quality factor of the close-loop circuit [10].

Consequently, the Q-enhancement techniques result from two approaches: physically adding a capacitor $c_q$ and electrically tuning Vbias2. Figure 3 shows that without adding $c_q$, the center frequency response of the second-order lowpass filter has a center frequency located at 2.48GHz and a Q equal to 2.4. In this paper, we compromise both approaches by choosing a capacitor value $c_q$ equal to 0.35pF with the tuning of Vbias2 together to reach a wide Q tuning range in highly spread center frequencies. By varying Vbias2 and Vbias3, the Q larger than 1000 with center frequency tunings between 1.26GHz and 2.3GHz are achieved with the addition of capacitor $c_q$=0.35pF. Figure 4 exhibits the Q variations from 10 to 1256 at the center frequency at 2.07GHz while all bias voltages remain except that only Vbias2 is tuned from 2.8V to 3.46V. The measured deviation of the center frequency in Figure 4 is 25MHz. If the low Q characteristic is required, then the value of $c_q$ must be reduced. Q equal to 1.2 can be obtained in the frequencies of interest.

## 3. NOISE ANALYSIS

Noise performance is another essential consideration that governs the filter design in communication applications. It determines the smallest input signal that the filter can effectively process. The input-referred thermal noise can be expressed as

$$\begin{aligned}\overline{v_{in\_LP}^2} &= 4\,k\,T\,R_s + \frac{8}{3}\,k\,T\,(\frac{1}{gm_1} + \frac{g_{m7}^2}{g_{m1}^2\,g_{m3}} \\ &+\frac{g_{m7}^2\,g_{m8}}{g_{m1}^2\,g_{m3}^2} + \frac{g_{m7}}{g_{m1}^2} + \frac{g_{m9}}{g_{m1}^2}) \qquad (4)\end{aligned}$$

In the above equation, $Rs$ represents the output impedance of the preceding stage, where a smaller of $Rs$ leads to better noise performance. In some cases, $Rs$ is fixed at 50Ω. We also note that the input-referred thermal noise can be minimized by properly adjusting the transconductance of the transistors: increasing $g_{m1}$; decreasing $g_{m7}, g_{m8}$, and $g_{m9}$. In addition, $g_{m3}$ must be simultaneously increased to maintain the same center frequency $\omega_o$ for fair comparisons, as indicated in Eq.2. The transistor M1 of the input stage plays a critical role in the input-referred noise representation, and a large transistor size W/L is required. For the same bias current, a better strategy of minimizing the transconductance is to increase the gate-to-source voltages of transistors M7, M8, and M9 without using large transistor sizes, and thus reduce the capacitive loading.

The linearity of a broad band filter can be tested by applying a single-tone signal so that the dominant harmonic terms fall into the passband of the filter without significantly attenuated by the frequency response of the filter.

A lowpass filter with a center frequency at 2.07GHz and Q equal to 31 is designed employing 0.5$\mu$m CMOS BSIM1 model to illustrate the feasibility of this filter configuration. The Q tuning range with a capac-

Table 1: The performance metrics of the lowpass filter.

| | |
|---|---|
| Capacitor Cq | 0.35pF |
| Center Frequency | 2.07GHz |
| Q | 31 |
| Q-tuning Range | 10 - 1256 |
| Maximum Input Swing for 1% THD | 18.4m$V_{rms}$ |
| Total Passband Noise (Voltage referred to input) | 0.123m$V_{rms}$ |
| Dynamic Range | 44dB |
| Power Dissipation | 27.8mW |

itor equal to 0.35pF is between 10 and 1256 by tuning Vbias2 exclusively. The total harmonic distortion (THD) is obtained by applying a 10MHz single-tone signal, and then observes the output spectrum. The maximum input voltage 18.4m$V_{rms}$ for 1% THD is obtained, and the total passband noise is 0.123m$V_{rms}$. Therefore, the input dynamic range is about 44dB and the power dissipation is equal to 27.8mW. The overall performance metrics are listed in Table 1.

## 4. CONCLUSION

CMOS low-Q and high-Q tunable second-order filter topologies for lowpass filtering have been analyzed, designed and simulated. The high-Q filter with a center frequency close to transistor $f_T$ is achieved by considering the distributed high frequency parasitic capacitance and characteristics of transistors as filter elements. Other parasitic poles and zeros along with lower principal complex poles largely contribute to the quality factor in the gigahertz filter design.

In the future, the temperature sensitivity of the center frequency and Q will be further investigated and analyzed.


## Acknowledgments

This project is sponsored by DARPA (Contract No. N65236-96-C-8607). The authors would like to thank Jeff LaCoss for his support.


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