

# Resonant Tunneling Transistors for Threshold Logic Circuit Applications

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## Abstract

*Resonant tunneling transistors (RTT's) and linear threshold gates based on monostable-bistable logic transition elements (MOBILE's) are promising candidates for nano-scale integrated circuits. In this paper the design methodology of RTT logic gates is discussed and experimental results of a monolithically integrated NAND-NOR gate are presented. To exploit the computational functionality of threshold logic circuits a depth-2 full adder and a bit-level pipelined ripple carry adder are proposed.*

## 1. RTT Circuit Design

In recent years different high speed logic families for resonant tunneling devices based on the MOBILE gate have been proposed and operated at clocking frequencies of several GHz [1], [3]. The MOBILE gate is a dynamic circuit and consists of two resonant tunneling diodes (RTD's) which are switched into a monostable or bistable state depending on an oscillating bias voltage (clock). For the circuit designer these gates are interesting to reduce the complexity of basic arithmetic building blocks by means of threshold logic or multiple-valued logic [2], [4].

In this work we investigate the design and application of threshold logic circuits using a modified MOBILE gate where the HFET input stage is replaced by RTT's. Basically, the RTT is a monolithically integrated three terminal InP-based RTD/HFET structure where the RTD is grown on the HFET drain contact [1]. For logic circuit applications the layer structure has been optimized to obtain a low peak voltage of  $V_p = 0.27$  V. If the RTD acts as current limiting device the RTT can be switched on and off by the gate voltage (fig.1(a)). In addition, the RTD peak current is independent of the gate voltage if a logic high level of  $V_H > 0.3$  V is applied.

Main intention of using an RTT input stage is the definition of a design parameter  $A$  to describe the ratios of the RTD areas in regard to the minimum area  $A_{min} = 10 \mu m^2$  because the logic function of a MOBILE gate depends on the

RTD peak currents. Especially if the gate has multiple input terminals the design parameter simplifies the translation of a given logic function into a circuit.

Based on this design methodology a dynamic NAND-NOR gate has been fabricated and tested (fig.1(b,c)). Assuming that the two input RTTs  $T_1$  and  $T_2$  have minimum dimensions, that is  $A = 1$ , we obtain a NAND function if the design parameter of the load RTD  $D_2$  is  $A = 2.5$  and a NOR function for  $A = 1.5$ . Fig.1(c) shows that the input and output voltage levels are compatible for a clock voltage of  $V_{CLK} = 0.77$  V and that the voltage swing of  $V_H - V_L = 0.65$  V is sufficiently large to switch the RTT's in a following circuit stage.

## 2. Threshold Logic Full Adder

The characteristic feature of linear threshold gates (LTG's) is the parallel processing capability of multiple inputs. The basic operations of a LTG are to compute the weighted sum of  $N$  digital input signals  $x_i$  and to generate a digital output  $y$  by a comparison with a given threshold value  $\theta$ :  $y = \text{sign}(w_1 x_1 + \dots + w_N x_N - \theta)$ .

The MOBILE concept allows a compact circuit implementation of a LTG where the inputs sum  $\chi$  corresponds to the current sum of the input RTT's. By combining this circuit architecture with a special threshold logic algorithm we have designed an efficient depth-2 full adder (fig.2(a)). The underlying idea of this algorithm is to exploit the periodical relationship between the sum bit  $s_i$  and the operand sum  $\chi = a_i + b_i + c_{i-1}$ . The first stage of the full adder contains three LTG's having the threshold values  $\Theta = \{1, 2, 3\}$  and classifies the operand sum according to the intervals shown in fig.2(b). Finally, the second stage detects whether the operand sum lies in one of the two high intervals  $\chi = [1, 2]$  and  $\chi = [3]$  or not. In terms of threshold logic equations the complete full adder is described by:

$$\begin{array}{ll} x_i(\chi) &= \text{sign}(a_i + b_i + c_{i-1} - 1) \\ \text{carry } c_i(\chi) &= \text{sign}(a_i + b_i + c_{i-1} - 2) \\ y_i(\chi) &= \text{sign}(a_i + b_i + c_{i-1} - 3) \\ \text{sum } s_i(\chi) &= \text{sign}(\chi - c_i + y_i - 1) \end{array} \quad (1)$$

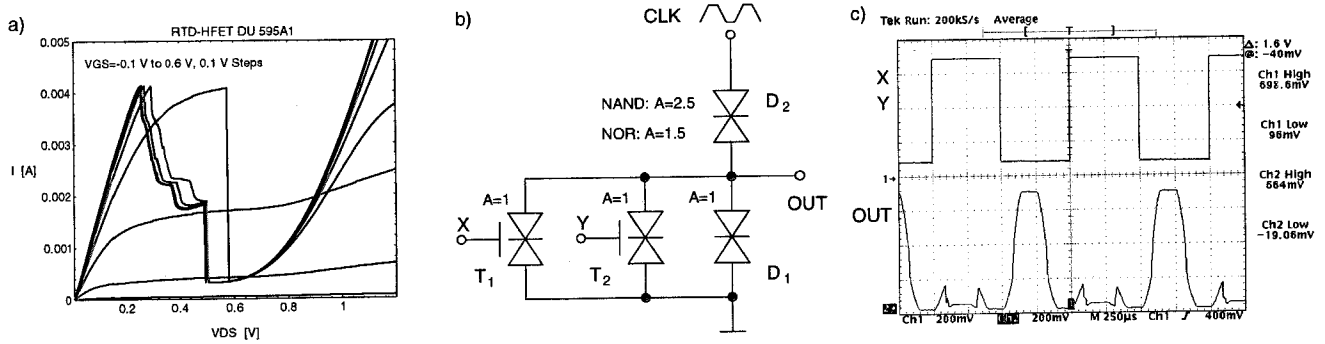


Figure 1. RTT I-V characteristics (a), MOBILE NAND/NOR logic gate (b), and measurement result (c).

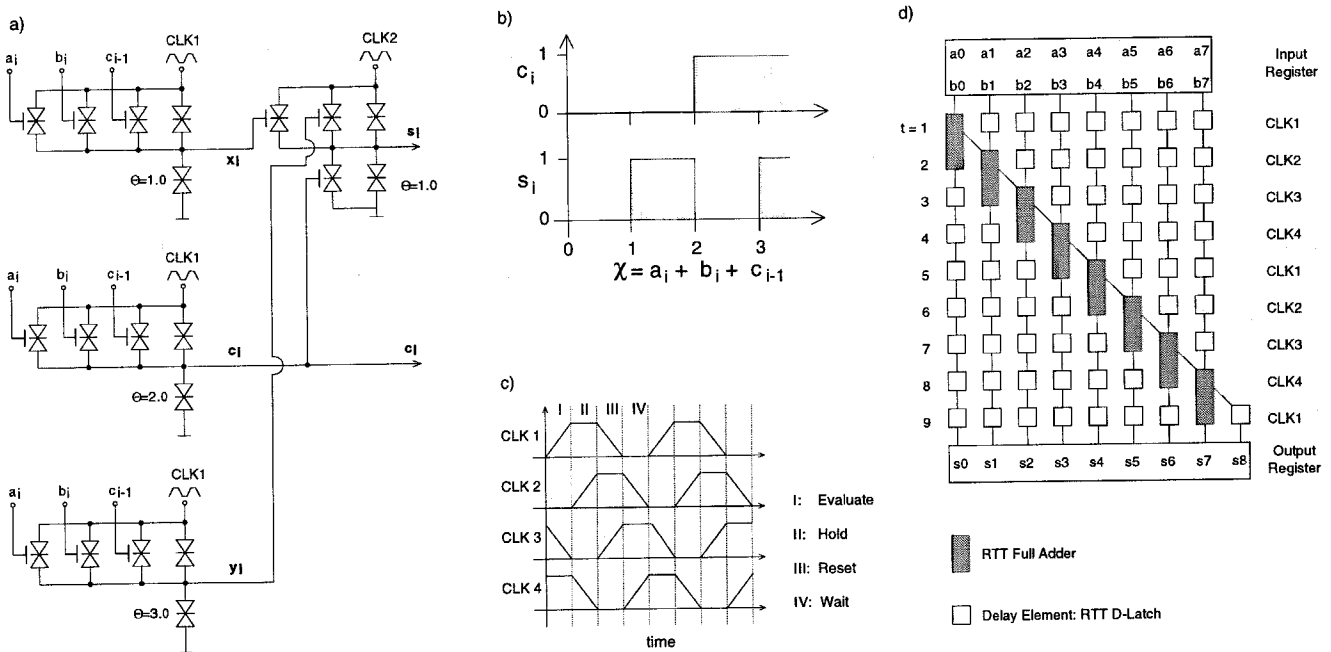


Figure 2. Full adder (a), threshold logic addition (b), four phase clocking scheme (c), and 8-bit RCA.

### 3. Bit-Level Pipelined Ripple Carry Adder

From the viewpoint of the circuit design MOBILE gates are edge triggered D-latches with an embedded logic input stage. Therefore, it is very attractive to operate the full adder in a bit-level pipelined fashion using an overlapping clocking scheme (fig.2(c)). The complete clock period  $T$  consists of four phases with a phase delay of  $T/4$  between each clock signal. This ensures that the evaluation of the sum bit in the second stage only starts after the first stage has finished the computation of  $(x_i, c_i, y_i)$ . For a pipelined  $n$ -bit ripple carry adder (RCA) the full adders are connected in such a way that the carries are propagated in diagonal direction (fig.2(d)). The time delay caused by the carry propagation is considered by delay elements. Thus, the operands  $a_i$  and  $b_i$  are arriving simultaneously with the carry  $c_{i-1}$  at the corresponding full adder. Due to the combination of

a bit-level pipelined architecture with threshold logic gates the  $n$ -bit RCA has a small latency of  $T_{add} = (n + 1)T/4$ . Moreover, since typical clocking frequencies of MOBILE gates are in the GHz range [3] high data throughput rates of 10 to 50 GBit/s are achievable with this circuit architecture.

### References

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