Assessing Defect Coverage of Memory Testing Algorithms

Vonkyoung Kim[1] and Tom Chen[2]
[1]Sun Microsystems 901 San Antonio Rd USUN02-302 Palo Alto CA 94303
[2]Electrical Engineering Dept Colorado St University Ft Collins CO 80523
(408) 774-8502 kvk@Eng.Sun.COM

Abstract

This paper describes the defect coverage evaluation of memory testing algorithms. Realistic CMOS defects were extracted from a 2 × 2 SRAM layout using an IFA tool, and circuit simulations were performed to measure the defect coverages of the eleven memory testing algorithms.

1 INTRODUCTION

The rapid development in memory technology demands new memory testing algorithms not only reducing the memory testing cost but also enhancing the defect detection capability, and therefore, the quality of the product. Abadir et al.[1] and van de Goor[2] introduced various ad-hoc memory testing algorithms. These ad-hoc algorithms, also referred to traditional algorithms, are designed to detect stuck-at faults. Other memory testing algorithms including March test are also proposed [2][3].

Although many memory testing algorithms claimed better fault detection capabilities compared to other testing algorithms, the real defect coverages of the memory testing algorithms are not clearly and accurately reflected by the functional fault coverage. Veenstra et al.[4] evaluated the fault coverage performances of various functional memory testing algorithms. Van de Goor[5] investigated the effectiveness of the March tests over the previous testing algorithms in terms of the fault coverage. Riedel et al.[6] measured functional fault coverages of several memory testing algorithms by generating and evaluating test patterns for a 3 × 3 memory array. All of the previous studies measuring the effectiveness of the memory testing algorithms used the functional fault coverage as the measure for test effectiveness. The functional fault coverage has some advantages in the sense that the functional fault models are developed to map the physical defects to make them easier to handle and understand. However, the functional fault coverage measure may not accurately reflect the effectiveness of the test with regard to the actual number of defects being detected. Furthermore, some of the defects in memory cells are difficult to be mapped to the set of functional faults.

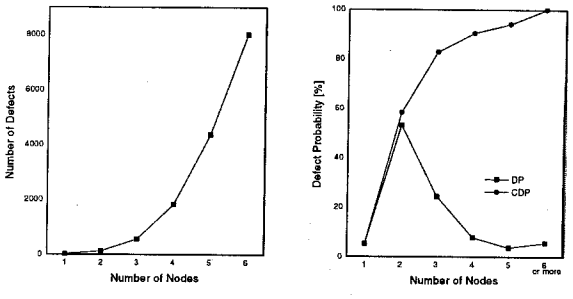

Fig 1. defect coverage of 2 × 2 SRAM array

In this paper, we propose a new approach to evaluate the coverage performance of the memory testing algorithms based on their physical defect coverages.

2 DEFECT COVERAGE

A 2 × 2 SRAM array layout designed using scalable 0.5μm CMOS process was used for analyzing possible defects in a SRAM array. An IFA tool[7] was used to extract the spot defects from the layout. The IFA is a procedure that determines the failures that can occur in a circuit due to the presence of a spot defect[8]. Figure 2 shows the number of possible defects and the defect probabilities versus the number of nodes to be considered for possible bridging. The number of defects increases exponentially with the increasing number of nodes involved in a bridge or a break. However the defect probabilities of multiple-node-defects are insignificantly low with the increase in the number of nodes involved in a bridge or a break(See Figure 2). In Figure 1, DP represents the defect probability with respect to the number of nodes, and CDP represents the cumulative defect probability. We limited the number of node

0-7695-0104-4/99 $10.00

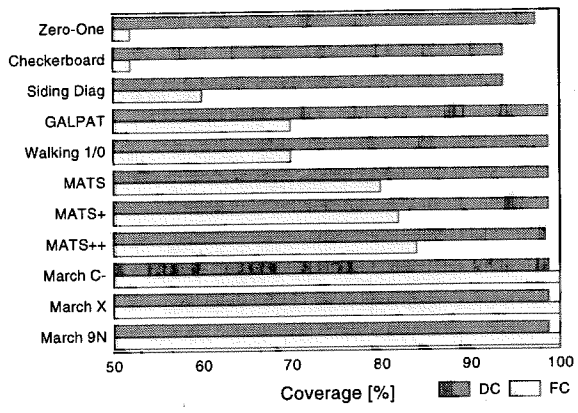

Fig 2. memory defect coverage result

upto five in order to lighten the simulation burden, while maintaining a high defect coverage(about 95%).

3 RESULT & DISCUSSION

Figure 2 summarizes the defect coverage evaluation results. The defect coverage results take the weighted defect probability into consideration, because each defect has its own probability reported by the IFA tool. Consequently, the defect coverage of a memory testing algorithm will be different to that of the other algorithm, even though the number of undetected defects is the same as the other. Figure 3 compares the defect coverage results with previously published functional fault coverage results[4][5] in a bar graph. In this graph, DC denotes the defect coverage and FC denotes the functional fault coverage.

We compared our results with previously published functional fault coverage results[4][5]. It is interesting that the two coverage metrics showed noticeable differences, especially for those algorithms commonly believed to have inferior coverages. The previous functional fault coverage results shows that the newer tests, including MATS and March tests, are much more effective than the older tests(ad-hoc or traditional test). However, our results showed that the effectivenesses of the newer tests and the older tests are about the same as far as the defect coverage is concerned.

4 CONCLUSION

The main goal of a test algorithm is screening bad parts by detecting physical defects. The functional fault models have been developed in order to handle the physical defects more easily, because the number of possible physical defects are enormously large in a large scale integration. However, the lack of defect coverage evaluation of the memory testing algorithms may result ineffective memory test strategy selection. We propose a new evaluation approach to measure the performance of the memory testing algorithms based on their physical defect coverage metrics. The defect coverage measures of eleven popular memory testing algorithms are evaluated using HSpice circuit simulation. The experimental result shows that the defect coverages of the eleven memory testing algorithms are not much different regardless of their complexities. As a conclusion, any known memory testing algorithm including primitive Zero-One test can provide an adequate defect coverage. However, it is also verified that the newer algorithms, such as March tests, have improved defect coverages than that of the ad-hoc tests. In order to increase the resolution of the defect coverage evaluation, a bigger size array is recommended. However, increasing the array size may cause very long circuit simulations due to the large number of possible defects.

5. ACKNOWLEDGEMENT

We would like to acknowledge Hewlett Packard Company for funding this research. We also appreciate Skip Roberts and Dr. Mick Tegethoff for their technical contribution to this research.

References

[1] M. Abadir and H. Reghbati, "Functional Testing of Semiconductor RAMs," *Comput. Surv.*, vol. 15, pp. 174–198, Sept. 1983.

[2] A. J. van de Goor, *Testing Semiconductor Memories.* John Wiley & Sons Ltd., 1st ed., 1991.

[3] R. Dekker, F. Beenker, and L. Thijssen, "A Realistic Fault Model and Test Algorithms for static random access memories," *IEEE Trans. Computer-Aided Design*, vol. 9, pp. 353–361, June 1990.

[4] P. K. Veenstra, F. P. M. Beenker, and J. J. M. Koomen, "Testing of random access memories: theory and practice," *IEE Proceedings, part G*, vol. 135, Feb. 1988.

[5] A. J. van de Goor, "Using March Test to Test SRAMs," *IEEE Design Test Comput.*, pp. 8–14, Mar. 1993.

[6] M. Riedel and J. Rajski, "Fault Coverage Analysis of RAM Test Algorithms," in *Proc. of VLSI Test Symp.*, pp. 227–234, 1995.

[7] A. Jee and F. J. Ferguson, "Carafe: An inductive fault anlysis tool for CMOS VLSI circuits," in *Proc. of VLSI Test Symp.*, pp. 92–98, 1993.

[8] J. Shen, W. Maly, and F. Ferguson, "Inductive Fault Analysis of MOS Integrated Circuits," *IEEE Design Test Comput.*, vol. 2, pp. 13–26, Dec. 1985.