Monolithic Microprocessor and RF Transceiver in 0.25-micron FDSOI CMOS

E. McShane, K. Shenai, L. Alkalai+, E. Kolawa+, V. Boyadzhyan+, B. Blaes+, and W. C. Fang+

Department of Electrical Engineering and Computer Science
University of Illinois at Chicago
1120 SEO, M/C 154
851 S. Morgan St.
Chicago, IL 60607
{emcshane,shenai}@eecs.uic.edu

+Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, CA 91109-8099
{Leon.Alkalai,Elizabeth.A.Kolawa,
Vardkes.Boyadzhyan,Brent.R.Blaes,
Wai-Chi.Fang}@jpl.nasa.gov

Abstract

A monolithic RFIC in 0.25-micron fully-depleted SOI CMOS has been designed consisting of a microcoded 8-bit 33-MHz microprocessor, a 400-MHz 8-bit ASK-modulated RF transceiver, and two integrated dc-dc voltage converters for power management. This architecture exploits a low-power (sub 2-V) digital process for mixed-signal VLSI in a die size measuring 2.2 mm x 2.2 mm.

1. Architecture and Performance

We have designed a monolithic RFIC consisting of digital, analog, and RF systems for a 2-V 0.25-micron fully-depleted (FD) SOI CMOS process for applications in wireless embedded control and remote sensing. It demonstrates the integration potential of a technology optimized for low-power digital circuits. The architecture (Fig. 1) consists of a digital processor core, an RF transceiver, an I/O interface linking the processor to communications, and two on-chip dc-dc voltage converters for integrated power management.

The digital core consists of an 8-bit 33-MHz CPU and a 256-byte SRAM for local program store and exercising the digital circuits. A reduced instruction set (Fig. 2) performs ALU operations and transfers between memory and RF I/O. I/O control is interrupt-driven, and a single shared register is used for data transfer (Fig. 3).

The zero-IF transceiver [1] uses an ASK modulation of eight baseband tones in a 100-kHz bandwidth for digital communications. Baseband signal recovery is achieved with parallel envelope detectors which translate the ASK modulation into a binary word (Fig. 4). The output of 8 parallel ring-oscillators is gated with a binary word to generate an ASK-modulated baseband signal (Fig. 5).

The 2-V supply and $V_{t0,n} \approx 0.5$ V decreased available internal signal swing and increased noise susceptibility for analog cells [2]. The operational amplifiers in this design achieved A_0=20,000 with a 3-dB BW≈250 MHz.

2. Physical Design and Fabrication

This IC was designed in a 2.2 x 2.2 mm footprint for the MIT/Lincoln Lab 0.25-micron FD-SOI CMOS process and is now in fabrication. It is part of an ongoing effort to integrate analog, RF, and digital circuits into a low-voltage digital technology [3]. Design methodologies developed in this effort will improve signal integrity and reduce turn-around time in future work.

Independent analog and digital power and ground rails were used to reduce injection of digital switching noise onto analog rails. Partitioning of analog and digital systems achieved minimal-length common edges within the layout. Also, sensitive analog blocks and signal lines were shielded by interconnect lines tied to independent "clean" grounds. Pin assignment and floorplanning were performed to minimize path lengths to pads and to separate analog and digital I/Os. The die floorplan and layout design are shown in Fig. 6. Analog/RF cells consumed approximately 80% of the die area.

3. Acknowledgment

This work was in part performed at the Center for Integrated Space Microsystems, Jet Propulsion Laboratory, California Institute of Technology. This was sponsored by the National Aeronautics and Space Administration.

References

[1] D. Shen *et al*, "A 900-MHz RF Front-End with Integrated Discrete-Time Filtering," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 1945-1953, 1996.

[2] E. Peeters *et al*, "A fully differential 1.5V low-power CMOS operational amplifier with a rail-to-rail current-regulated constant-gm input stage," in *Proc. Custom Int. Circ. Conf.*, 1997, pp. 75-78.

[3] E. McShane *et al*, "Monolithic Microprocessor and RF Transceiver for Low-Power Mobile Applications," in *SPIE AeroSense*, 1998, pp. 20-28.

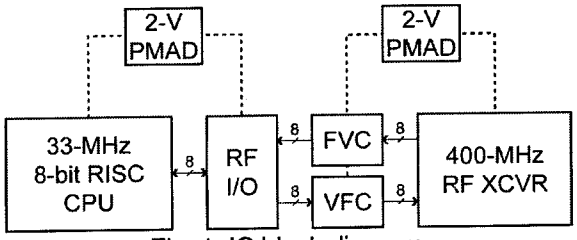


Fig. 1 IC block diagram.

		4	2	2
R-Type		opcode	rs	rd
ADD	R1, R2	R1 <- R1 + R2		
SUB	R1, R2	R1 <- R1 - R2		
AND	R1, R2	R1 <- R1 ^ R2		
XOR	R1, R2	R1 <- R1 ⊕ R2		
SLL	R1, R2	R1 <- R1 << R2		
SLT	R1, R2	R1 <- ? (R1 < R2)		
SEQ	R1, R2	R1 <- ? (R1 == R2)		
MOVI2S	SPR, R1	SPR <- R1		
MOVS2I	R1, SPR	R1 <- SPR		
LB	R1, R2	R1 <- M[R2]		
SB	R1, R2	M[R2] <- R1		
JALR	R1	R3 <- PC + 1; PC <- R1		

		4	4
I-Type		opcode	immediate
LI	#15	R0 <- 15	
BEQZ	name	? (R0 == 0) PC <- PC + name	
TRAP	name	IAR <- PC; PC <- name	
RFE		PC <- IAR	

Fig. 2 Instruction set architecture.

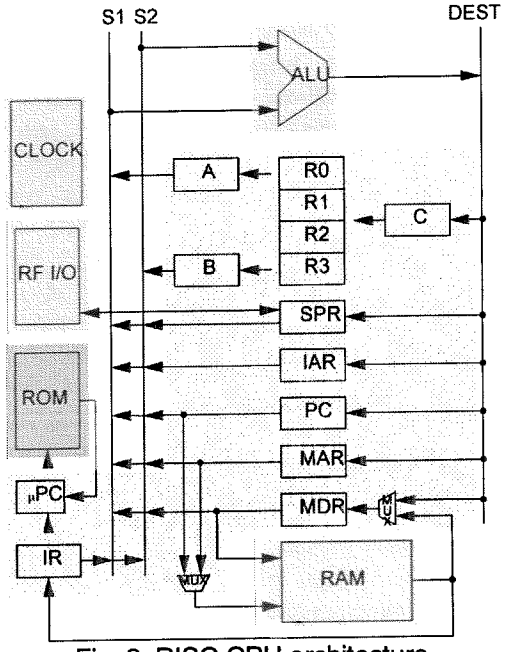


Fig. 3 RISC CPU architecture.

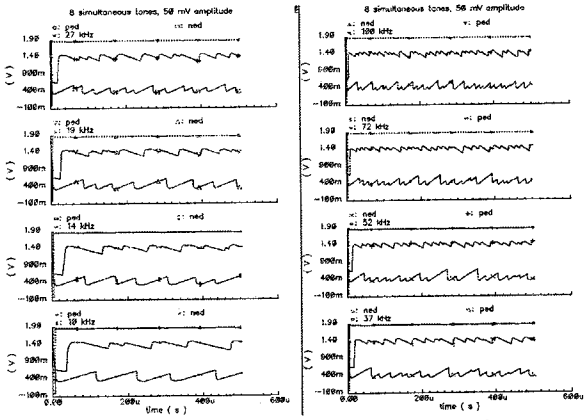


Fig. 4 Transient response of envelope detectors.

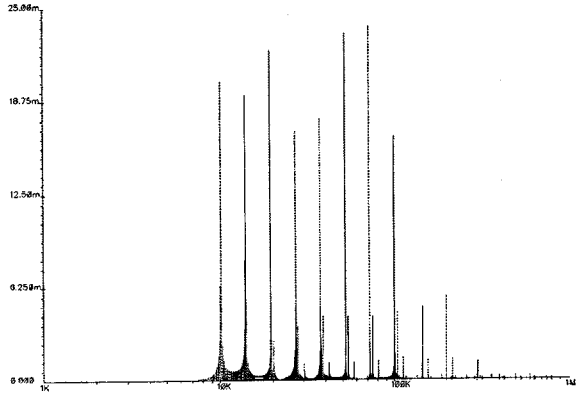
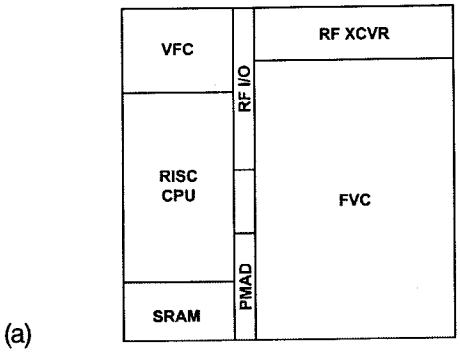
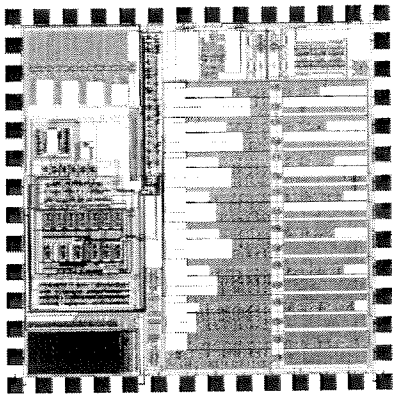


Fig. 5 Frequency spectrum of baseband data tones.



(a)



(b)

Fig. 6 RF microsystem (a) floorplan and (b) layout.