NMOS Energy Recovery Logic

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Abstract

In this paper, we describe NMOS Energy Recovery Logic (NERL) which exhibits high throughput with low energy consumption due to efficient energy transfer and recovery using adiabatic and bootstrapping. NERL shows full output voltage swing, insensitivity to output load capacitance, less dependency on power-clock frequency and complementary outputs for balanced capacitance load to power-clock. We have designed an 8-bit CLA and inverter chain using 0.6μm CMOS technology and verified that NERL saves energy over ECRL by 2 to 3 times.

I. Introduction

Power dissipation has become a critical concern in both high performance and portable applications due to limited battery life and reliability of integrated circuits. The increasing demand for low-power very large scale integration (VLSI) can be addressed at several levels, namely, the algorithmic, architectural,circuit, and process technology levels. In this paper we will consider circuit level techniques for low-energy computation using adiabatic logic.

Adiabatic logic uses an AC power-clock source which is used for both power and clock. The input and output of adiabatic logic gates should be complementary to have a constant, data-independent capacitive load to the clock in order to maintain a constant oscillation frequency. Several adiabatic logic circuits have been proposed and their potential for practical applications has been shown [1] – [6]. Gabara [2] proposed a Pulsed Power Supply CMOS circuit. It requires latches and its stored energy is not fully recovered. Hinman et al. presented Recovered Energy Logic using bipolar transistors, but it is not a complementary structure and is a ratioed logic [3]. Adiabatic logic using diodes or diode-connected MOSFETs, such as the 2N-2N2D as shown in Fig. 1(a), dissipates energy proportional to the threshold voltage, thus placing a lower bound on the efficiency of these circuits [3]–[5], and can have only degraded logic levels. Efficient Charge Recovery Logic (ECRL) proposed by Moon and Jeong shown in Fig. 1(b) uses cross-coupled PMOS transistors instead of diodes [6]. Although it avoids energy dissipation due to diodes, energy is not completely recovered and its energy dissipation is highly dependent on the output load capacitance.

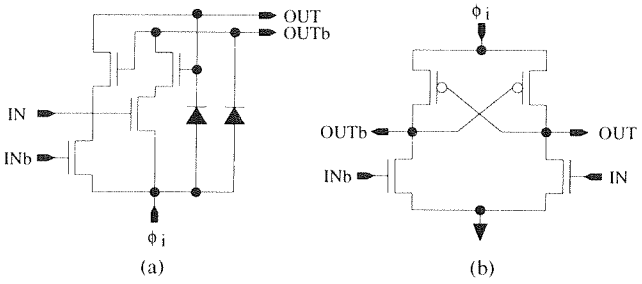

Figure 1: Inverters using: (a) 2N-2N2D and (b) ECRL

We propose an NMOS Energy Recovery Logic (NERL) family which uses bootstrapping for maximum energy transfer and full output voltage swing. These circuits feature full rail-to-rail logic swing, insensitivity to load capacitance, and significant energy saving over previous adiabatic logic circuits.

This paper is organized as follows. Section 2 describes the basic operation of NERL and gives comparison results of the energy dissipation. In section 3, we discuss design issues and present the energy consumption of 8-b adders for conventional logic and NERL. Conclusions are finally drawn in section 4.

II. NMOS Energy Recovery Logic Family

Basically, all NERL gates use complementary inputs and outputs to balance load capacitances for each power-clock. NERL gates use only NMOS transistors, which reduces chip area. NERL uses bootstrapping for full energy recovery, pass-transistors for logic function, and 4-phase power-clocks for shorter latency. Although the speed of each NERL gate is relatively low, the throughput of the system using NERL is high because of the inherent pipelining of adiabatic logic circuits.

A. NERL Inverter

The basic NERL inverter circuit is illustrated in Fig. 2. It is composed of two main parts, the bootstrapping and the logic function. Bootstrapping circuit consists of bootstrapped NMOS transistors (M7, M8) with two isolation transistors (M5, M6). The logic circuit consists of four pass-transistors (M1~M4). M9 and M10 ensure stable

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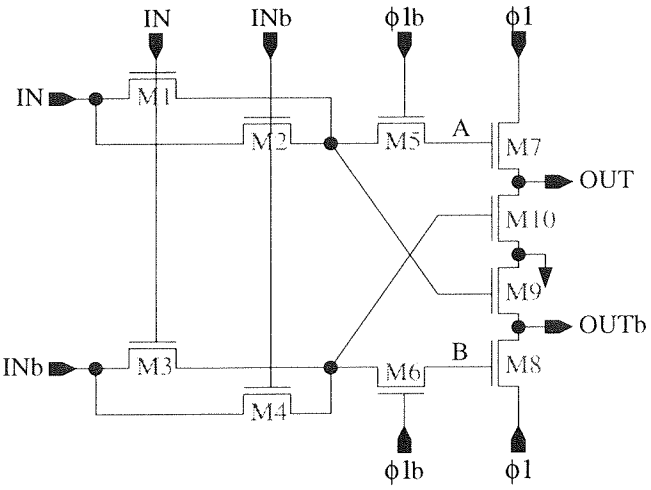

Figure 2: NERL inverter

operation by preventing the floating of the output nodes. Two power-clock signals with a 180° phase difference are used for each logic gate. Power-clock ϕi is for transferring charge from the power-clock to the output nodes. The other power-clock ϕib is for precharging a bootstrapping node (A or B depending on its inputs) and keeping its voltage level high enough to transfer charge completely and recover the used charge fully. Next two power-clock signals follow with a 90° phase lag for pipelining, respectively. Simulated timing diagram and node voltage waveforms of an inverter are shown in Fig. 3. A clocking rule must be followed to form a chain of logic circuits. Each clock is followed by the next clock with a 90° phase lag for a complete pipelined operation.

The AC power-clocks can be sinusoidal waveforms. For convenience, we use trapezoidal waveforms here. Before evaluation, all output nodes are set to ground through either M7(or M10) and M8(or M9). During the first period, t1, power-clock ϕ1b ramps from 0 to V_p(peak voltage of power-clock) to turn on isolation transistors (M5, M6) before the synchronized inputs to power-clock ϕ2b arrive. The combination of inputs and connections of pass-transistors decide which bootstrapping node will be precharged. In case of Fig. 3, input signal, IN, rises high during t2 and turns on M1, precharging bootstrapping node A to $V_p - V_{th}$. INb remains low which results in keeping bootstrapping node B at low. These inputs come from previous stages in the cascaded architecture.

As the power-clock ϕ1 goes up, the gate of transistor M7 is bootstrapped to a voltage well above V_p due to the gate-to-channel capacitance of M7. The charge, hence, is passed from ϕ1 to output node, OUT, with maximum energy-transfer efficiency.

When ϕ1 ramps down, energy stored in output nodes are recovered fully through M7 in the adiabatic manner during t4 period, because node A is isolated from the input signals after ϕ1b goes down to ground. Charge at node A remains, keeping M7 turned on. As shown in Fig. 3, the output of the first cascaded inverter, OUT, comes after a quarter

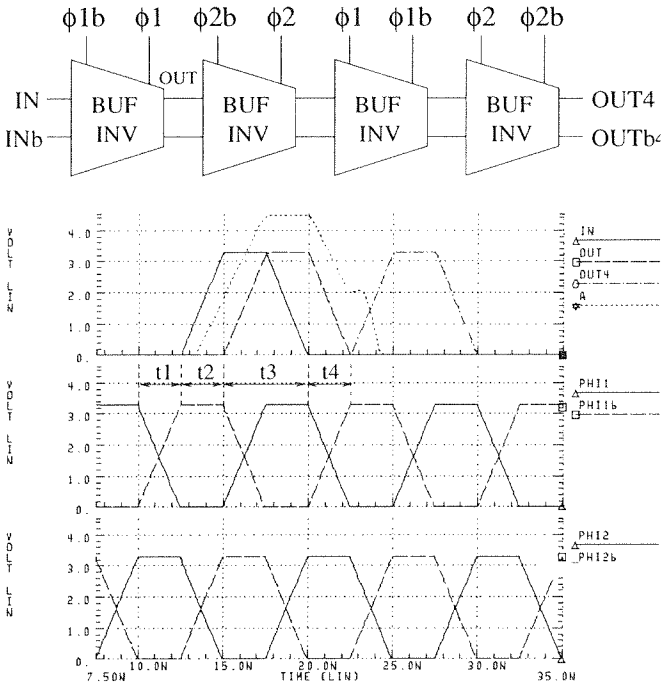

Figure 3: 4-phase power-clocks and simulated timing waveforms of NERL inverter chain

cycle of power-clock latency, and the output of the fourth, OUT4, after one cycle.

B. Energy Dissipation

Energy dissipation of logic circuits is compared in this section. First, the conventional CMOS logic dissipates energy as follows

$$E_{CMOS} = C_{load} V_{dd}^2 + E_{short} \quad (1)$$

where C_{load} is the load capacitance, and E_{short} is energy dissipation due to the short circuit current during the transition. Turned-on MOS transistor can be modeled as a resistor. The potential across the resistor dissipates energy and no energy is recovered to the power source in CMOS logic.

Adiabatic logic keeps the potential across the switching devices small using AC power source. Energy to the power source is recovered during the discharging phase. Even though the energy consumption in adiabatic logic is much smaller than that of the conventional CMOS, adiabatic logic using diodes or diode-connected MOSFETs for precharge [1] – [2] cannot avoid energy consumption due to the voltage drop across the diode when turned on. Although ECRL can avoid energy consumption due to such voltage drop across the diode, the full energy recovery through PMOS transistor is not achievable. The energy dissipation in ECRL is [6]

$$E_{ECRL} = \frac{1}{2} C_{load} V_{tp}^2 + E_{ope} \quad (2)$$

where V_{tp} is the PMOS threshold voltage, and E_{ope} is energy dissipation due to latch operation during logic compu-

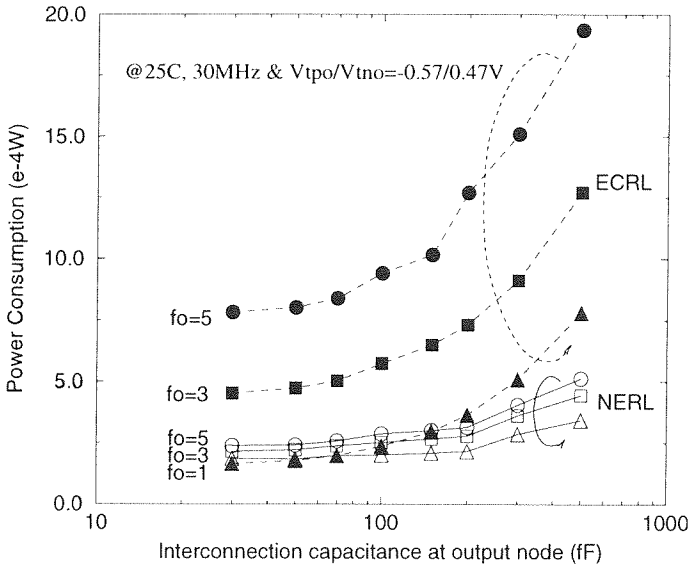

Figure 4: Power consumption comparison of inverter chains with various fanouts and interconnection capacitances

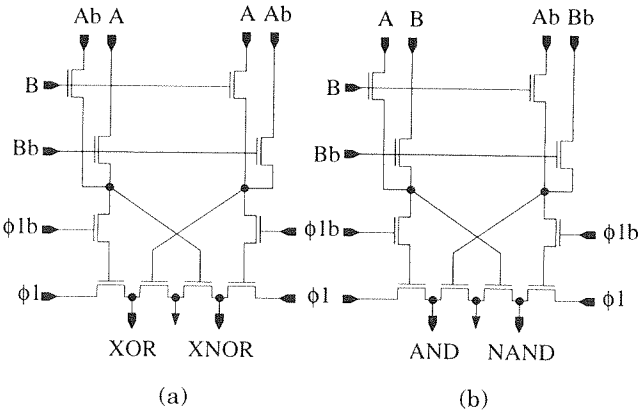

Figure 5: NERL gates: (a) XOR/XNOR and (b) AND/NAND

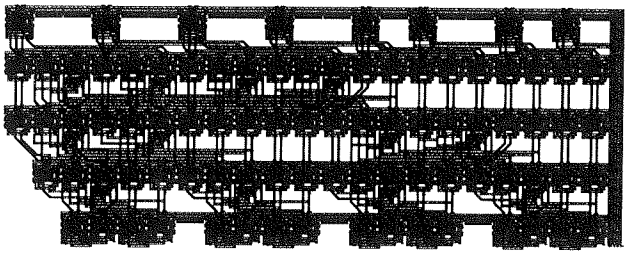

Figure 6: Layout of an 8-b adder using NERL

tation in ECRL. Because NERL transfers energy between power-clock and output node completely, energy dissipation is only due to precharging of bootstrapping nodes through isolation transistors during t2 shown in Fig. 3. Its energy dissipation can be written as

$$E_{NERL} = C_{boot} V_p V_{tn} + E_{opn} \quad (3)$$

where C_{boot} is the capacitance of bootstrapping node, V_{tn} is the threshold voltage of the isolation transistor, and E_{opn} is the energy dissipation due to non-adiabatic precharging of the bootstrapping nodes. Energy dissipation is lowered significantly, because the capacitance of the bootstrapping node is much smaller than that of output node.

Fig. 4 illustrates the HSPICE simulation results of energy consumption comparison of inverter chains using proposed circuits and ECRL with optimized transistor sizes. Compared to ECRL inverter chain, NERL inverter chain dissipates far less energy at all interconnection capacitances and fanouts except small interconnection capacitance under fanout 1. NERL saves much energy especially for large load interconnection capacitance with large fanout.

C. Complex Gates and Other Gates

Although the XOR is the logic function with the least efficient implementation in CMOS and ECRL, NERL XOR has the same circuit topology as NERL inverter except several connections. Fig. 5(a) shows the XOR/XNOR gate in NERL circuit topology. As shown in this figure, NERL complex gates can be implemented with few pass-transistors. All basic gates such as inverter, multiplexer, NOR, XOR and NAND shown in Fig. 5(b) have the same topology. The only difference among basic NERL gates lies in several node connections. Therefore, design automation using proposed circuit can be achieved easily and similarly to that of differential pass-transistor logic (DPTL) [7].

III. System design

A. Digital IC

The inherent wave-pipelined structure of the power-clock distribution provides several advantages for the proposed circuit design. While the delay per gate is big compared to the conventional CMOS gate, the throughput of NERL system is high because the throughput of adiabatic system is proportional to the speed of power-clock, independent of logic depth. Therefore, for the systems with large logic depth, significant energy savings can be achieved without loss of throughput. Furthermore, the latency of NERL system using 4-phase power-clock is 4 times smaller than 2N-2N2D system using a 2-phase non-overlapping power-clock. It has been known that the clock system and the logic part consume almost equal amount of power in various CMOS chips, and the clock system consumes 20% to 45% of the total chip power [8]. Power consumption due to glitches also cannot be ignored in CMOS. But, in adiabatic logic, there is no additional power consumption due to clocking and glitching.

Adder is an essential and basic building block in digital system. Therefore, we have designed and laid out an 8-bit carry-lookahead adder using 0.6μm CMOS technology to show the efficiency of the proposed circuit design

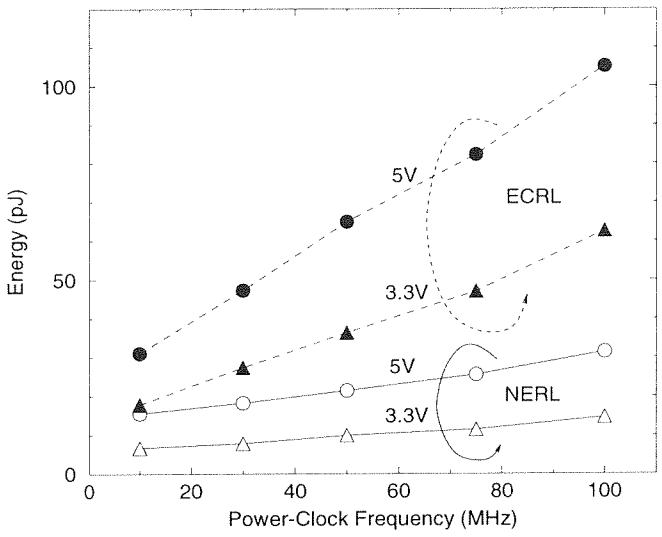

Figure 7: Energy comparison of 8-b adders

in actual applications. The number of transistors used to implement this adders is 492 for ECRL and 898 for NERL. Fig. 6 shows the layout of an 8-bit adder using NERL. Although the NERL adder uses more transistors than the ECRL adder, both occupy almost equal die area, the NERL adder occupies 0.11 mm^2 and the ECRL adder, 0.10 mm^2. The reason for this is that NERL does not need n-wells for PMOS transistors and uses only small transistors for the logic and isolation part. Adders and multipliers using ECRL dissipates 3 to 4 times less energy than CMOS[9]. As illustrated in Fig. 7, the 8-bit adder using the proposed circuit design consumes 2 to 3 times less energy than the ECRL adder over various power-clock frequencies and power supply voltages. The latency of this adder using NERL is only one cycle of the power-clock.

B. Mixed-Signal IC

There has been an increasing need for mixed-signal integrated circuits. An on-chip Analog-to-Digital converter (ADC) and Digital-to-Analog converter (DAC) are desired that has greater than 10-bit accuracy for the future multimedia applications. In order to accommodate such high-performance analog and digital functions on a single-chip, it is critical to reduce the coupling of digital noise to analog circuits.

Adiabatic logic can use sinusoidal waveforms instead of the square waveforms. NERL, hence, is a good candidate for digital logic in mixed-signal IC. Often, noise coupling from digital section to analog section is a serious problem. Analog circuits that are integrated with digital circuits have digital noise coupling problem and the techniques for its avoidance are very needed. Digital noise coupling are due to capacitive coupling, coupling through the power supply, and coupling through the substrate. NERL reduces these digital noise because the digital section using NERL does not incur high frequency harmonic noise nor flows high short-circuit current during transition. Proposed circuit, hence, can be used especially within low-power large-bit ADC and DAC.

IV. Conclusions

We have proposed a new NMOS Energy Recovery Logic (NERL) which exhibits high throughput with low energy consumption due to efficient energy transfer and recovery using bootstrapping. NERL also shows full output voltage swing, insensitivity to output load capacitance, less dependency on power-clock frequency, and complementary outputs for balanced load capacitance to power-clock. We designed an 8-bit CLA and inverter chains using 0.6μm CMOS technology to verify the area and performance efficiency of NERL in real applications. Simulation results showed that an adder using the proposed circuit design consumes 2 to 3 times less energy than an ECRL adder at various frequencies and peak power supply voltages. Design automation using the proposed circuit architecture can be achieved easily because of its regular topology. NERL is a good low-power digital logic candidate in mixed-signal IC as well as in digital IC.

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