

No-race Charge-recycling Differential Logic (NCDL)

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Abstract

This paper describes No-race Charge-recycling Differential Logic (NCDL) which realizes low power computation with less sensitivity to input signal skews. Performance comparison with previous charge recycling logics is shown for a 2-input NAND logic. NCDL operates in push-pull mode and achieves about 35% improvement in power-delay product over full swing differential logic without the pre-evaluation problems. Thus, it shows increased effectiveness for the implementation of random logic with input signals arriving in an arbitrary sequence.

1 Introduction

Energy efficient circuit design is one of the crucial requirements for future consumer devices. Conventional dynamic circuit techniques are mostly aimed at high speed operation rather than low power consumption. Several charge recycling differential logic techniques have been proposed to realize low power computation with high noise margin. They use a charge sharing technique to recycle part of the used charge for precharge. Under ideal conditions, they can reduce power consumption up to 50% compared to conventional dynamic logics.

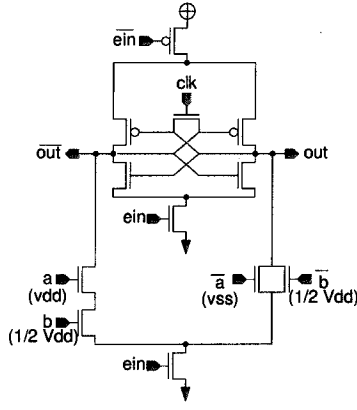
Kong, *et al.* [1] have proposed Charge Recycling Differential Logic(CRDL) for this purpose. In this technique, PMOS transistors whose threshold voltages are higher than half V_{dd} are required to eliminate conducting paths from V_{dd}

to output nodes during a precharge phase. High threshold PMOS transistors are achieved by applying a higher voltage ($\geq 20V$) than V_{dd} to the N-well bias. Additionally, CRDL suffers from a pre-evaluation problem in a particular implementation.

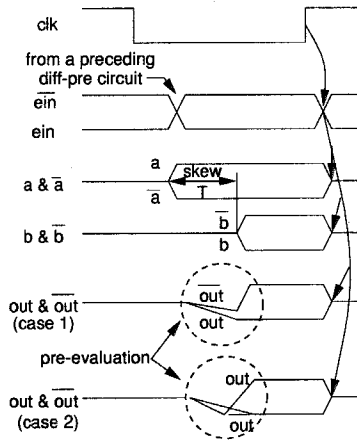
Choe, *et al.* [2] have suggested Half-Rail Differential Logic(HRDL) to soothe the pre-evaluation problem in a chain of logic where evaluation takes place with a ripple effect. The control circuit is inserted between the differential-precharge (diff-pre) circuits (i.e., logic evaluation part) to activate the following diff-pre circuit after the evaluation of the preceding stage is completed. Even though HRDL solves the pre-evaluation problem in some cases, it is not freed from the problem completely when there are skews in signals for the following diff-pre circuit. Skew is due to different sources from which control signals and input signals originate.

We have developed a new charge recycling logic which realizes low power computation without the pre-evaluation problems seen in other previous charge recycling logics. The new logic operates in push-pull mode and shows stable operation with significant improvement in power-delay product over conventional dual-rail dynamic logic.

This paper is organized as follows. In Section 2, the circuit concept and operation are discussed. In Section 3, simulation results for 2-input NAND logic are shown. Finally, Section 4 presents our conclusions.



(a) diff-pre circuit for 2-input NAND HRDL



(b) timing conditions for pre-evaluation

Figure 1: Diff-pre circuit for 2-input NAND HRDL and timing conditions for pre-evaluation

2 Circuit Concept and Operation

Fig. 1 shows the diff-pre circuit used to implement 2-input NAND function by HRDL and timing conditions for the pre-evaluation case. In the evaluation phase (clk is low), if one of input signals arrives with time skew (T) after the diff-pre circuit is activated by ein and $\overline{ein}$, the diff-pre circuit may experience the pre-evaluation problem as shown in Fig. 1(b). This is because both NMOS logic trees have conducting paths. Input signal conditions during skew time (T) are also presented in Fig. 1(a). According to the degree of signal skews and implemented functions, the diff-pre circuit may experience either pre-discharging (case 1) or wrong-evaluation (case 2). The pre-

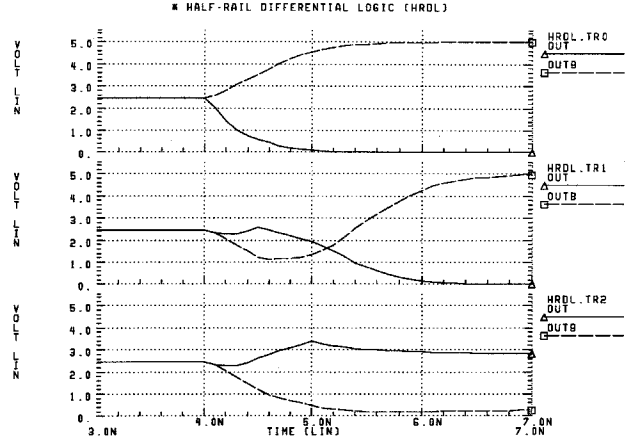


Figure 2: Output waveforms of 2-input NAND HRDL for input signal skews, 0, 0.5 & 1.0ns

evaluation problem becomes worse for larger input signal skews and/or logic function requiring to stack large number of transistors such as 4-input NAND logic. The pre-evaluation results in increase of power consumption and degradation of logic speed to some degree and sometimes in fatal malfunctions.

Fig. 2 shows HSPICE output waveforms of 2-input NAND HRDL for various input signal skews. Unlike the case without input skew (first row), the pre-evaluation occurs for 0.5ns input skew (second row) and the desired logic evaluation can not be performed for 1ns input skew (third row). Besides the pre-evaluation problem due to signal skews, the charge used for ein and $\overline{ein}$ is not recycled as shown in Fig. 1(b). Therefore, charge recycling efficiency is reduced when the fanout of the control circuit increases.

In this paper, we propose No-race Charge-recycling Differential Logic (NCDL) to achieve low power consumption without the pre-evaluation problem of the previous charge recycling logics.

2-input NAND function implemented by NCDL and timing diagram with signal skews are shown in Fig. 3. NCDL is composed of three parts, logic evaluation part (M1~M8), precharge part (M9~M13) and logic restoring part (M14~M21). NMOS complementary logic or PMOS complementary logic or CMOS

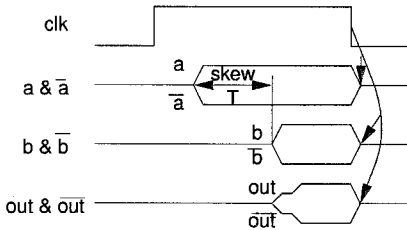
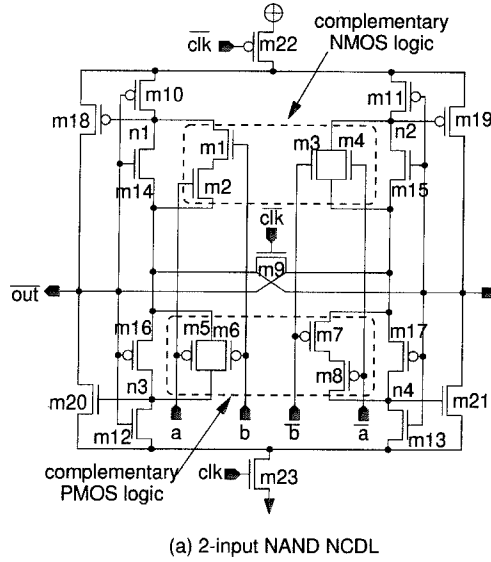


Figure 3: 2-input NAND NCDL and timing diagram

(NMOS & PMOS) complementary logic or pass-gate logic can be used for logic evaluation part. Like other precharged dynamic logics, the NCDL needs two phases for operation. In the precharge phase, clk and $\overline{clk}$ are low and high, respectively and NCDL is isolated from the supply. out and $\overline{out}$ are precharged to about $V_{dd}/2$ through M9. All input signals are also precharged to about $V_{dd}/2$ by other preceding stages. After clk goes high, M10~M13 are turned on since their gates are precharged to about $V_{dd}/2$ and n1 and n2 nodes are set to V_{dd} and n3 and n4 nodes to V_{ss} . So, logic restoring transistors (M18~M21) are turned off. Other transistors (M1~M8 & M14~M17) are also in a turned-off state since each gate-to-source bias is below the threshold voltage. Therefore, output nodes are in a high-impedance state and the precharge voltage is

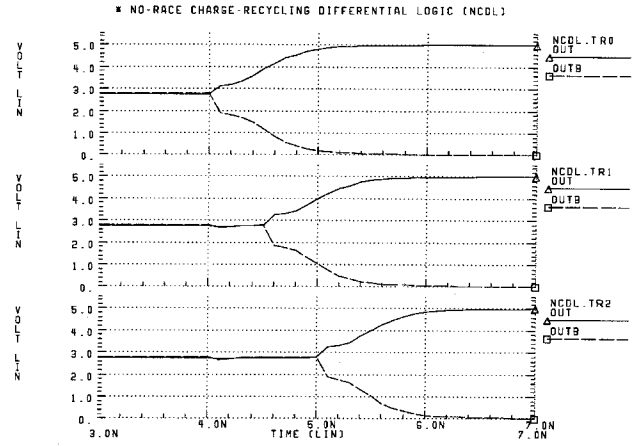


Figure 4: Output waveforms of 2-input NAND NCDL for input signal skews, 0, 0.5 & 1.0ns

maintained before input signals arrive. When input signals, a and $\overline{a}$, are developed by a preceding stage, M2 and M8 are turned on. But during other input signals, b and $\overline{b}$, remain at their precharged levels (i.e., these signals are not evaluated by a preceding stage yet), M1, M3, M6 and M7 are still turned off. When input signals, b and $\overline{b}$, arrive after signal skew time (T), M1 and M7 are turned on and logic evaluation starts. Therefore, the pre-evaluation problem in previous recycling logics cannot happen and valid evaluation is always performed in NCDL. After all input signals arrive, M1, M2, M7 and M8 are turned on and out is charged up to $V_{dd} - V_{tn}$ and $\overline{out}$ is discharged to V_{tp} , where V_{tn} and V_{tp} are NMOS and PMOS threshold voltages, respectively. These developed out and $\overline{out}$ voltages turn on M15 & M16 and M19 & M20 in sequence and logic levels are restored in full strength as shown in Fig. 3(b).

Fig. 4 shows output waveforms of 2-input NAND NCDL for different input signal skews. NCDL is free of the pre-evaluation problem even when the input skew is 1.0ns (third row).

3 Results

Table 1 compares 2-input NAND DCVS [3], HRDL and NCDL at above simulation points. P_{avg} is defined as average power measured at 40MHz operating frequency and delay is time

Table1. Summary of 2-Input NAND DCVS, HRDL & NCDL

Logic	# of tr.	Skew=0			Skew=0.5			Skew=1.0		
		Pavg	Delay	P*D	Pavg	Delay	P*D	Pavg	Delay	P*D
DCVS	13	242.9	0.91	221.0	243.6	1.42	345.9	244.0	1.91	466.0
HRDL	18	108.2	1.03	111.4	329.2	2.19	719.8	N.A.	failed	failed
NCDL	23	124.1	1.12	139.0	126.4	1.60	202.3	126.0	2.08	262.1

(Pavg:uW, Delay,Skew : ns, P*D : fJ)

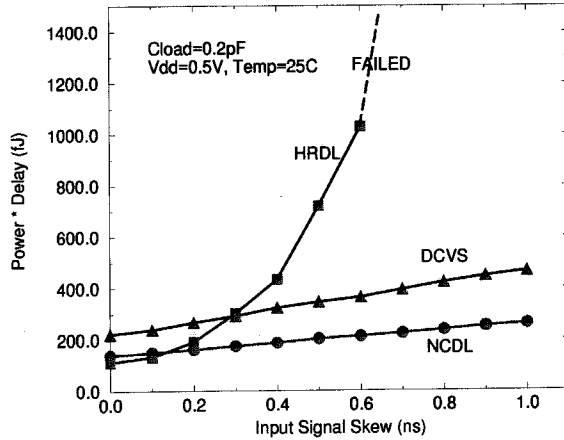


Figure 5: Power-delay product of 2-input DCVS, HRDL and NCDL for input signal skews

from when the first input signal is enabled to when output signal difference is reached to $0.8 \cdot V_{dd}$. Input signals are raised with the slope of 0.05ns/V . CRDL is excluded from comparison since it requires an additional control variable such as high well bias voltage. NCDL shows higher power-delay product than HRDL under ideal conditions. This is because NCDL consists of more transistors than HRDL, which results in larger gate capacitance and has dual logic evaluation steps which causes slightly longer intermediate states due to the time required for restoring transistors to start to act.

Fig. 5 shows power-delay product of 2-input DCVS, HRDL and NCDL for different input signal skews. NCDL is less sensitive to input signal skews and is guaranteed to have stable operation under real environment while HRDL shows great

performance degradation as input signal skews increase.

4 Conclusions

We have proposed NCDL to realize low energy computation without the pre-evaluation problems seen in previous charge recycling logics. The operation and characteristics of NCDL are verified by HSPICE simulations for various designs. NCDL is a push-pull type logic and about 35% of power-delay product can be improved over conventional dual-rail dynamic logic. NCDL shows increased effectiveness for function logics requiring higher stacked transistor structures and under real chip environment with input signal skews. Thus, NCDL makes it possible to implement random logic without extra design overhead.

References

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