Integration of InAs/AlSb/GaSb Resonant Interband Tunneling Diodes with Heterostructure Field-Effect Transistors for Ultra-High-Speed Digital Circuit Applications

P. Fay, G. H. Bernstein, D. Chow†, J. Schulman†, P. Mazumder‡
W. Williamson*, and B. Gilbert°

Department of Electrical Engineering, University of Notre Dame,
275 Fitzpatrick Hall, Notre Dame, IN 46556
voice: (219) 631-5693, fax: (219) 631-4393
email: pfay@nd.edu

† HRL Laboratories, 3011 Malibu Canyon Road, Malibu, CA 90265

‡ Department of Electrical Engineering and Computer Science, University of Michigan, 1301 Beal Avenue, Ann Arbor, MI 48109

* Institute for Defense Analysis, 1801 N. Beauregard St., Alexandria, VA 22311

° Mayo Foundation, Rochester, MN 55905.

ABSTRACT

Resonant tunnelling diode based logic circuits offer significant advantages for low power, ultra-high-speed applications. In this work, a low-power resonant interband tunneling diode (RITD)-based logic technology capable of operating at clock rates of at least 12 GHz is reported. The circuits are fabricated using InAs/AlSb/GaSb RITDs. Fanout of at least two at a clock rate of 10 GHz is also reported for two AND gates in a two-stage pipelined configuration. Simulation results for an RITD/HFET circuit based on measured characteristics of InAs/AlSb/GaSb RITDs and InAs-channel HFETs for a simple inverting Schmitt trigger are presented to demonstrate the advantages of an integrated RITD/HFET technology. This circuit architecture demonstrates proper operation with power supply voltages as low as 0.5 V. In addition, well defined logic levels and abrupt logic transitions are achieved, despite the limited transconductance and large output conductance typical of InAs-channel HFETs.

Keywords: resonant tunneling diode (RTD), resonant interband tunneling diode (RITD), heterostructure field-effect transistor (HFET), ultra-high-speed logic circuits

INTRODUCTION

New approaches to device and circuit design are required to accommodate the continuing push toward faster circuits for digital signal processing applications. One approach to achieving multi-Gb/s logic functionality is to leverage the extremely high device speeds of resonant tunneling diodes (RTDs). RTDs have been shown to operate with switching times as low as 1.5 ps [1]. In addition to their intrinsically high speeds, the unique current-voltage characteristics of RTDs, which feature a well-defined peak and substantial negative differential resistance, can be used to greatly reduce the circuit complexity required to realize logic functions [2-4]. As a consequence of the reduced number of devices required, the speed of logic functions using RTD-based logic is further enhanced. Power consumption of RTD-based logic circuits is also small; RTD-based logic gates with power dissipations of 0.5 mW per gate operating at 12 GHz have been demonstrated [5], leading to logic switching energies as low as 41.7 fJ.

An important variation on the RTD device structure that has the potential to further increase the performance of RTD-based circuits is the resonant interband tunneling diode (RITD). This structure takes advantage of the unique broken-band alignment present in InAs/AlSb/GaSb heterostructures. Figure 1 shows simplified schematic en-

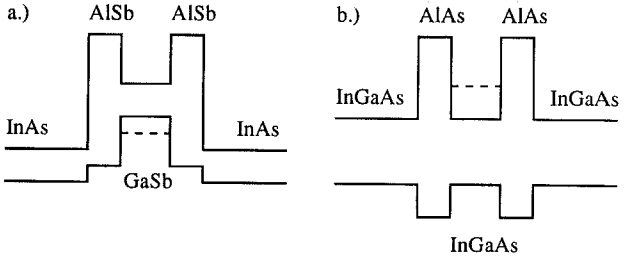

Figure 1. Schematic energy band diagrams for (a) RITD and (b) conventional RTD structures.

ergy band diagrams for both RITD and conventional RTD structures. An important consequence of the broken-band alignment in the RITD structure is that electrons tunnel from the conduction band in the emitter through the AlSb barrier, through a valence band state in the well, and into the conduction band in the collector. One result of this interband process is a significant shift in the observed current-voltage characteristics for RITDs compared to RTDs, whereby RITDs have considerably lower peak and forward voltages than conventional RTDs. Because of these lowered characteristic voltages, circuit designs with lower operating voltages and correspondingly lower power consumption can be achieved using RITDs.

A further extension of the benefits of RTD-based circuits can be achieved by using a technology that permits incorporation of FETs as well as RTDs in the circuit. The additional design flexibility afforded by including FETs in the circuit include increased output drive current levels, increased logic fanout, and improved output-to-input isolation. For successful integration of FETs with RTDs, a compatible material system for both FETs and RTDs must be selected. For conventional RTD-based circuits, integration of InP-based RTDs and heterostructure FETs (HFETs) have been demonstrated [6]. RITDs, however, depend critically on the broken-band alignment that can be achieved with heterojunctions between AlSb and GaSb. For this reason, HFETs based on the InAs/AlSb/GaSb material system have been selected. In addition to material system compatibility with RITDs, HFETs in this material system benefit from the very high electron velocity and sheet concentration achievable in InAs quantum wells. Despite the relative immaturity of this material system, excellent device speeds have been achieved in HFETs based in this material, further indicating its potential for use in ultra-high-speed electronic systems [7]

In this work, the operation of RITD-based logic circuits at clock rates of at least 12 GHz is reported, and fanout of at least 2 at a clock rate of 10 GHz is demonstrated with two series-connected AND gates forming a two-stage pipelined circuit. Development of an integrated RITD/InAs-channel HFET process is ongoing; circuit applications and anticipated performance will be discussed for this RITD/HFET technology.

RITD-Based Logic Circuits

The N-shaped current-voltage characteristic inherent to RTDs permits compact realization of complete logic functions using RTDs [2-4, 8]. Figure 2 shows experimental current-voltage characteristics of an InAs/AlSb/GaSb RITD fabricated in our laboratory [9]; as can be seen in the figure, this typical device achieves a very low peak voltage of 0.12 V and a forward voltage of 0.61 V. This allows bistable circuit operation with power supply voltages of well under

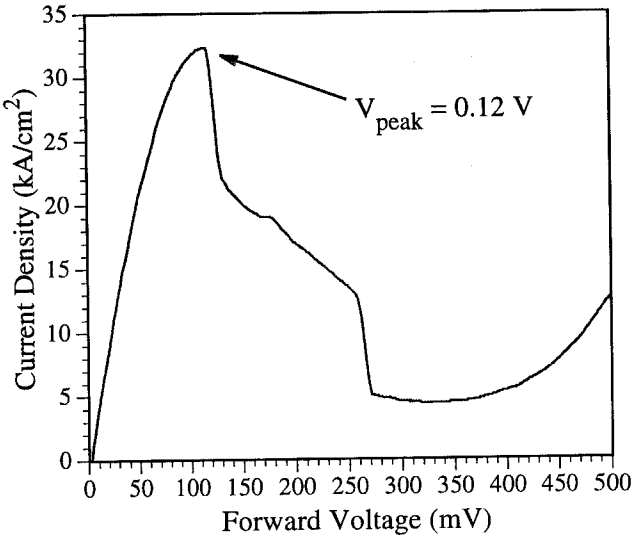

Figure 2. Experimental current-voltage characteristics of an InAs/AlSb/GaSb RITD.

1 V, and hence low power consumption.

One circuit architecture for realizing a logically complete family of gates using only RITDs and Schottky diodes has been demonstrated [5]. Figure 3 shows a schematic diagram of an exclusive-or (XOR) gate consisting of Schottky diodes and RITDs. (As described in [4], the specific logic functionality of the circuit is determined by the relative areas of the Schottky diodes and RTDs; a complete logic family can be effected by suitable choice of device area.) These devices were monolithically integrated in a stacked heterostructure in which the RITD layers were grown first, followed by the Schottky contact layer. This circuit was fabricated, and demonstrated correct logic functionality at clock rates of up to 12 GHz, which was the limit of the available test equipment. Measured input and output waveforms demonstrating the exercise of this circuit operating at a clock rate of 12 GHz are shown in Figure 4. The top trace in the figure is the 12 GHz clock, the middle traces are the two logic inputs; the bottom trace is the output of the RITD-based exclusive-OR gate. From the figure, the operation of the gate as a clocked exclusive-OR operating with a clock

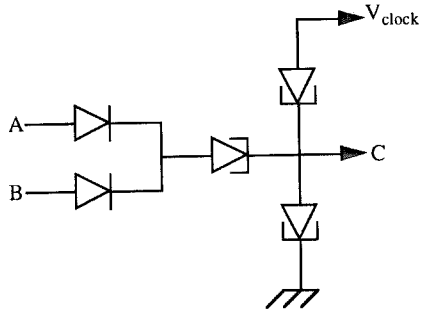

Figure 3. Schematic diagram of an exclusive-or (XOR) gate consisting of Schottky diodes and RITDs.

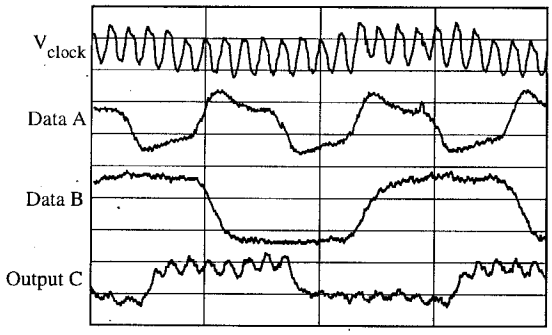

Figure 4. Measured input and output waveforms at a clock rate of 12 GHz.

rate of 12 GHz is verified. Operating speed of the RITDs is especially important in this realization of an exclusive-OR circuit since the state of two RITDs must switch within one clock cycle for proper operation. Therefore, Figure 4 suggests that the RITDs used in this circuit are capable of switching at speeds of at least 24 GHz.

To demonstrate fanout and high-speed operation simultaneously, the same circuit architecture as used for the exclusive-OR was used to implement two AND gates in a series-connected, pipelined configuration. The schematic circuit diagram for the pipelined gate is shown in Figure 5, and Figure 6 shows a die photo of the finished integrated circuit. The experimental results demonstrating operation at a clock rate of 10 GHz are shown in Figure 7. For pipelined operation, a two-phase clock (shown as the top two traces in Figure 7) is employed, with phase 1 clocking the first stage, and the second stage clocked with the second phase. This circuit, in addition to demonstrating the flexibility of this circuit architecture, also demonstrates a fanout of two; the output of the first AND gate in the pipeline feeds directly both inputs of the second-stage AND gate, and proper operation at a clock rate of 10 GHz is clearly obtained in Figure 7.

RITD-HFET Logic Circuits

One limitation of the circuit architecture demonstrated by the diode-based logic circuitry is in the dependence on

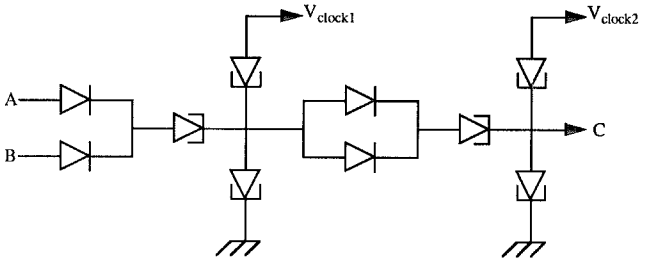

Figure 5. Schematic circuit diagram of two-stage pipelined AND logic gates using RITD-based logic.

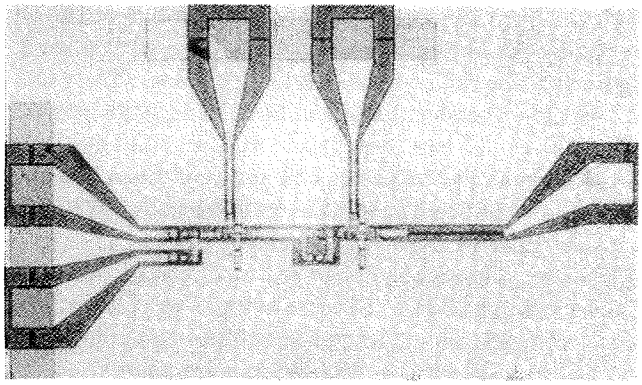

Figure 6. Die photo of completed two-stage pipelined series-connected AND gates.

the clock signal for supplying current for the individual logic gates. By adding HFETs, fanout can be increased and the need for power input from the clock is eliminated. Figure 8 shows a simple implementation of an inverting Schmitt trigger that is possible with a single HFET and RITD. The low peak voltage and forward voltages of the RITD are advantageous for this circuit since the required power supply voltage is lowered; in this case, well-defined logic levels are demonstrated with a power supply of 0.5 V. This is particularly advantageous for InAs-channel HFET-based technology due to the low drain bias limits of InAs-channel HFETs that are imposed by the onset of impact ionization.

In addition to its potential for low-power logic, this circuit clearly demonstrates the tremendous potential for reducing circuit complexity that is possible with RITD-based logic; a CMOS realization of an inverting Schmitt trigger (e.g. CD40106) requires 12 MOSFETs, as opposed to the single RITD and HFET in this implementation. Figure 9 shows the voltage transfer characteristic of this Schmitt trigger obtained from circuit simulation using the measured

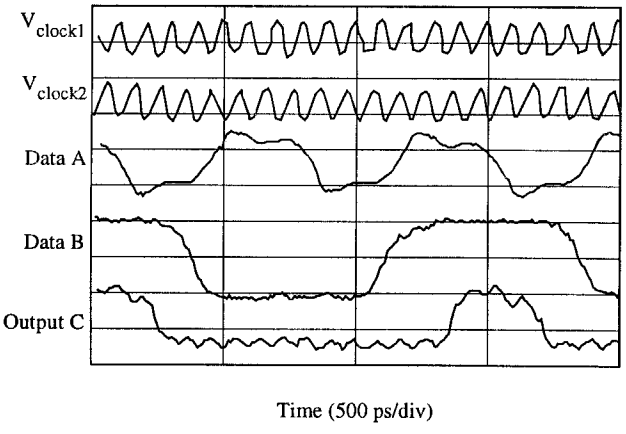

Figure 7. Measured input and output waveforms at a clock rate of 10 GHz for the two-stage pipelined AND gates. Proper operation with a fanout of two for the first stage is achieved.

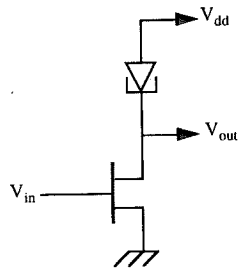

Figure 8. Circuit schematic for RITD/HFET Schmitt trigger.

current-voltage characteristics for the RITD from Figure 2 and a typical model for InAs-channel HFETs [10]. For the simulation, a large-signal dc model for a 1 μm gate length InAs channel HFET is used; this device has a peak transconductance of 320 mS/mm, an output conductance of 60 mS/mm, and a threshold voltage of -1.1 V. Despite the large output conductance of the InAs-channel HFET and low g_m/g_o ratio, abrupt high-low and low-high output transitions are obtained due to the strong negative differential resistance of the RITD. In addition, the bistability of the RITD provides the needed hysteresis for Schmitt trigger action; the width of the hysteresis is governed by the transconductance (and thus width and gate length) of the HFET and the peak-to-valley ratio of the RITD. For HFETs of fixed gate length and a fixed RITD heterostructure design, the hysteresis width is controlled by the ratio of HFET width (W) to RITD area (A). The simulation results shown in Figure 8 are for a W/A of 10 μm^{-1}; smaller hysteresis can be achieved by selecting a larger W/A ratio.

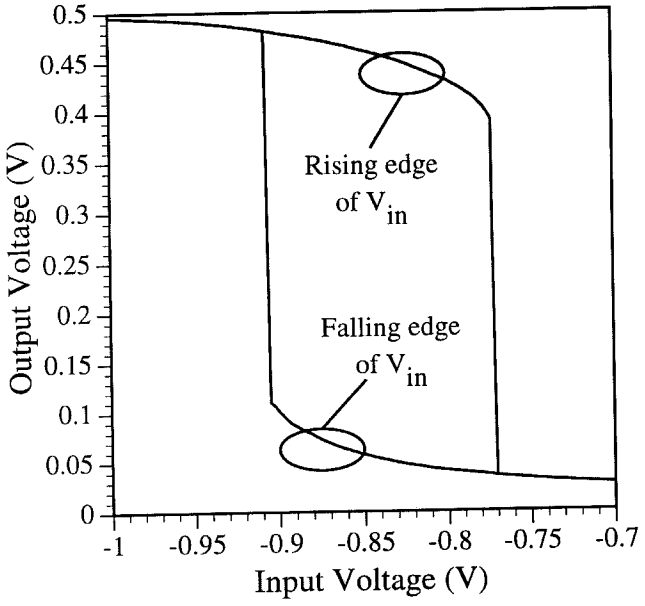

Figure 9. Simulated voltage transfer characteristic for RITD/HFET Schmitt trigger circuit. Abrupt output transitions are achieved even with large HFET output conductance typical of short gate-length InAs-channel HFETs.

Conclusions

The advantages of RTD-based circuits for low power, ultra-high-speed logic applications are discussed. A low-power RITD-based logic technology capable of operating at clock rates of at least 12 GHz is reported. Fanout of at least two at a clock rate of 10 GHz is also demonstrated experimentally for pipelined AND gates. Simulation results of an integrated RITD/HFET inverting Schmitt trigger circuit based on measured characteristics of RITDs and InAs-channel HFETs are presented. A significant reduction in circuit complexity is achieved compared to CMOS, and the circuit architecture demonstrates well defined logic levels and extremely abrupt logic transitions despite the limited transconductance and large output conductance typical of InAs-channel HFETs.

Acknowledgement

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