

Resonant Tunneling Technology for Mixed Signal and Digital Circuits in the 10-100 GHz Domain.

T. P. E. Broekaert, B. Brar, F. Morris, A. C. Seabaugh, G. Frazier
Raytheon Systems Company
Dallas, TX 75243
t-broekaert@rtis.ray.com
Phone: (972)-344-3611

Abstract

The inherent bistability and picosecond time-scale switching of the resonant tunneling diode (RTD) provides an ideal element for the design of digital circuits and analog signal quantizers in the 10-100 GHz domain. New differential RTD-based circuits for quantizers and a first-order Sigma-Delta modulator capable of operating at 10 GHz and beyond are introduced.

1. Introduction.

Resonant tunneling diodes have recently been integrated into a variety of low-power multi-GHz monolithic circuits. Demonstrations have included logic [1], frequency dividers [2], shift registers [3], low power memory [4], and analog-to-digital converters [5,6,7].

To attain high speed of operation and ease of scaling we have focused on combining the RTD with submicron gatelength, high f_t , high electron-mobility transistors (HEMTs). In this large-scale integration RTD-HEMT technology we have demonstrated: a 4-bit, 3 GHz analog-to-digital converter, a 3 GHz (50 dB spur free dynamic range) clocked quantizer, a 3 GHz sample & hold (55 dB linearity), clock circuits, shift registers, and low power SRAM (50 nW/bit). Other circuits of interest include mux/demux, true time delay, direct digital synthesizers, and fiber receiver functions with 10-100 GHz data rates.

To date most RTD circuit demonstrations have been single ended designs of subcircuits such as shift registers and quantizers. Here, the RTDs are applied to new differential versions of subcircuits to achieve a higher speed of operation and better noise immunity.

Previously, a differential RTD-based clock generator has been proposed [8] and demonstrated [9] based on four RTDs in a bridge configuration. The speed of the RTD-bridge can be exploited in other subcircuits as well. Applying the RTD-bridge to the design of quantizers and other latched logic circuits yields subcircuits with a higher speed of operation as compared to the single-ended designs, as will be discussed in sections 2 and 3.

The differential RTD-quantizer is also easily integrated into Sigma-Delta modulators. The advantage of the RTD-based quantizer in a Sigma-Delta modulator is that one can achieve a higher maximum sampling rate than in a quantizer design without RTDs. With the multi-GHz sampling rates enabled by the RTD-bridge quantizer the sigma-delta modulator then becomes a viable ADC architecture for the digitization of GHz signals.

2. Differential Quantizer

As a first approach to differential design, Figures 1 and 2 show two possible extensions of the single-ended quantizer demonstrated in Ref. [5]. Both versions transform the binary single-ended quantizer into a ternary differential design. The three logic states (-1, 0, +1) of the quantizer correspond to the RTD bias states of the negative bias "valley" region, the (positive and negative bias) "pre-peak" region, and the positive bias "valley" region. If the RTD I-V is not symmetric and symmetry is desired in the ternary quantizer then a symmetrized RTD can be realized by combining RTDs in parallel connected in opposing polarity ("anti-parallel").

For the differential quantizer shown in Figure 1 the RTD is reset through shunting with a FET switch. The RTD in the source of the input transistors is used only as a resistor for the purpose of linearizing the performance in *e.g.* a flash-type ADC. The current-source loads at the output are optional and remove any quiescent current from the RTD loads. The advantages of the RTDs carrying only the differential current are larger device parameter margins in matching the RTD and FET as well as symmetric biasing of the RTD.

For the differential implementation in Figure 2 the RTD also carries only the differential current. In this case, the RTD is reset through self-discharge with a

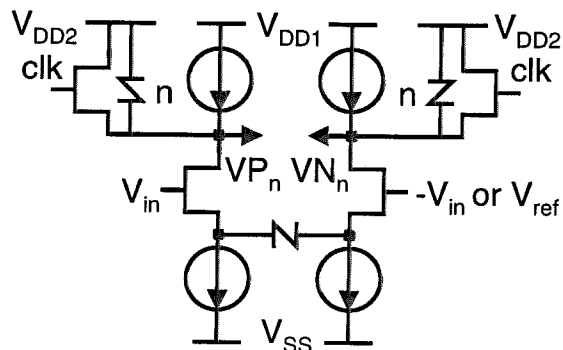


Figure 1. Ternary differential RTD-quantizer with FET-shunt reset. The current-sources at the output set the RTD common mode current to zero and are optional.

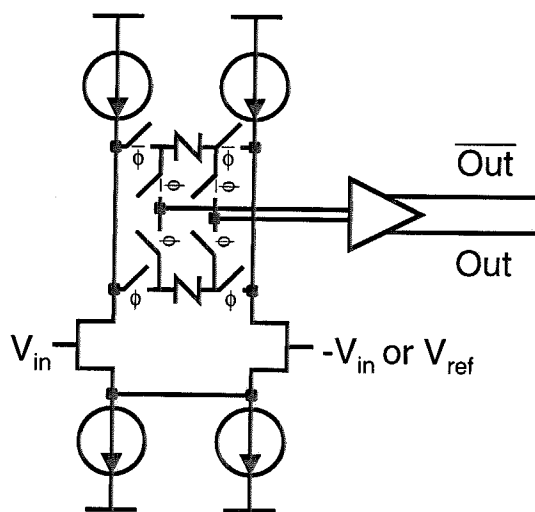


Figure 2. Ternary differential RTD-quantizer with FET-series reset. The sampling frequency is made twice the clock frequency by adding a second RTD switched on the opposite phase clock.

FET-series switch. The FET-series switch also enables doubling of the sampling frequency of the quantizer in a "ping-pong" architecture by adding a second RTD operated on the opposite phase clock.

The quantizer in both the FET-shunt and FET-series differential design operates in a ternary mode, allowing for the detection of two levels with a single differential circuit and halving the component count as compared to a conventional FET-only binary quantizer.

In simulation, for a transistor f_t of 100 GHz and an RTD with a peak current density of 50 kA/cm², the quantizer shown in Figure 1 operates at 25 Gsps while the quantizer of Figure 2 with the double RTD configuration operates at 50 Gsps. Although these differential designs offer improved noise immunity, reduced power supply switching noise, and increased speed of operation over single-ended designs one drawback is that they are still limited in maximum frequency of operation by the use of FET switches.

The following section describes a novel design that avoids the FET switch to achieve an even higher speed of operation.

3. RTD-bridge Quantizer

A very simple and compact differential-current comparator can be realized by combining four RTDs in a bridge configuration. In its simplest form, as shown in Figure 3, the RTD-bridge is driven by two transconductance amplifiers to obtain a ternary quantizer. The principle of operation of the bridge is as follows. Initially all RTDs are assumed pre-peak. The currents are split evenly with clock and signal currents adding or subtracting respectively in the four branches of the bridge. As the clock current is ramped up toward the peak current two opposing RTDs in the bridge will trip to the valley once the peak current is reached. The signal current required to trip the RTDs is $|I_{sig,t}| = 2 I_{peak,RTD} - I_{clock,max}$. The three states of the bridge (-1, 0, +1) then correspond to $-|I_{sig,t}| > I_{sig}$, $-|I_{sig,t}| < I_{sig} < +|I_{sig,t}|$, $I_{sig} > +|I_{sig,t}|$.

Since the bridge makes a decision each time the clock bias current is applied, independent of the clock bias polarity, 2 samples are taken for each clock period. As an additional advantage the bridge can be clocked with a sinusoidal clock signal thereby eliminating the need to carry higher order harmonics in the clock distribution network. Also note that the resulting output signal is of the return-to-zero (RZ) type with zero being at the center of the output ± 1 signals, enabling easy clock-recovery in data-communications circuitry.

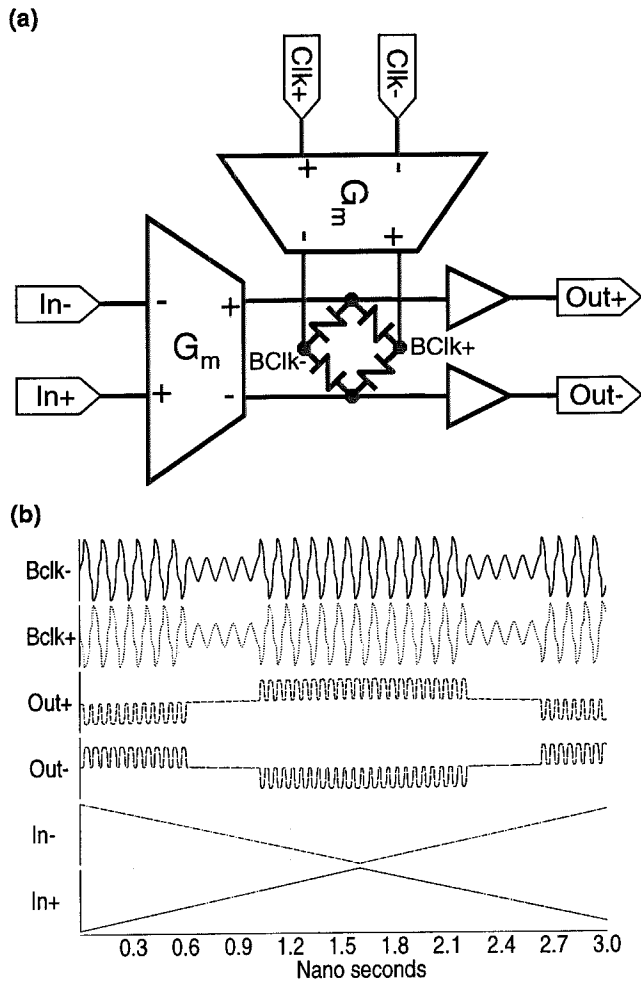


Figure 3. Ternary differential RTD-bridge quantizer. (a) Shows the schematic diagram and (b) shows a SPICE simulation at 20 Gsps (10 GHz clock). Shown are: the clock signals at the bridge, the output signals at the bridge, and the input signals.

If a binary quantizer were desired one could set $I_{\text{clock,max}}$ to $2 I_{\text{peak,RTD}}$, however, this would result in a design that is very sensitive to process variations and clock amplitude. The addition of a fifth RTD to the bridge, as shown in Figure 4, is a better method for achieving binary operation. The purpose of the fifth RTD across the clock inputs is to prevent the second pair of RTDs from tripping after the first pair has tripped by absorbing the excess clock current drive.

Assuming the same HEMT-RTD technology as in section 2 the SPICE simulated performance of the bridge based quantizer with a FET based transconductance amplifier shows mV level sensitivity at 10 Giga-sample-per-second operation and functionality up to 70 Gsps (35 GHz clock). A digital shift register based on the

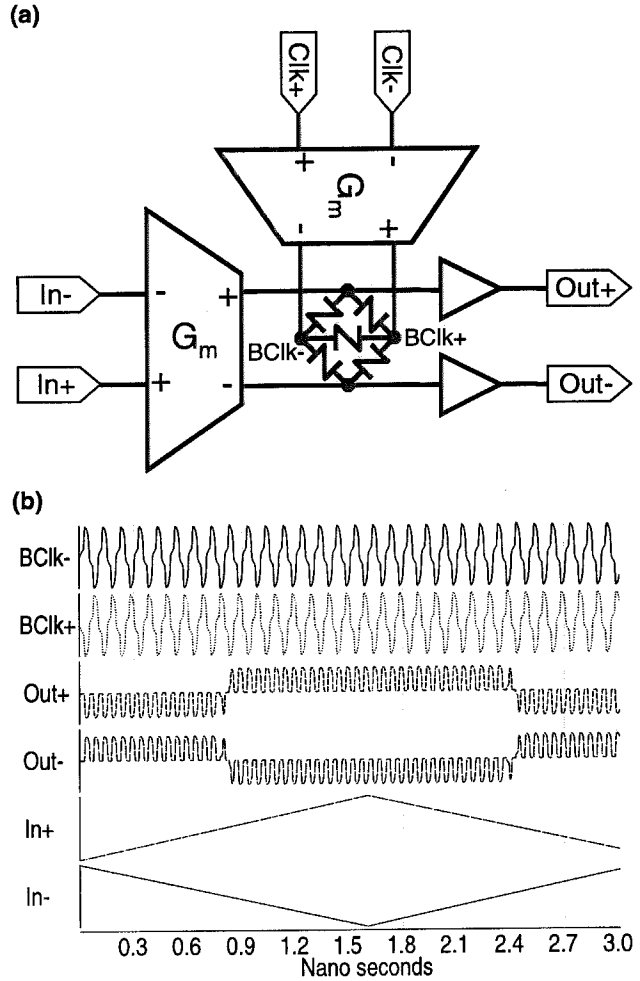


Figure 4. Binary differential RTD-bridge quantizer. (a) Shows the schematic diagram and (b) shows a SPICE simulation at 20 Gsps (10 GHz clock). Shown are: the clock signals at the bridge, the output signals at the bridge, and the input signals.

RTD-bridge is also functional up to 70 GHz data-rate shift operation. With increases in HEMT f_t beyond 100 GHz and RTD peak current density beyond 50 kA/cm², both within reach of laboratory-demonstrated devices, data-rates of 100 GHz and higher are expected to be achieved in the HEMT-RTD technology.

The quantizers as described in this section can be used as building blocks for latches, shift registers, and analog-to-digital converters.

4. Sigma-Delta Modulator

The RTD-bridge quantizer is also easily integrated into a Sigma-Delta modulator. For example, Figure 5

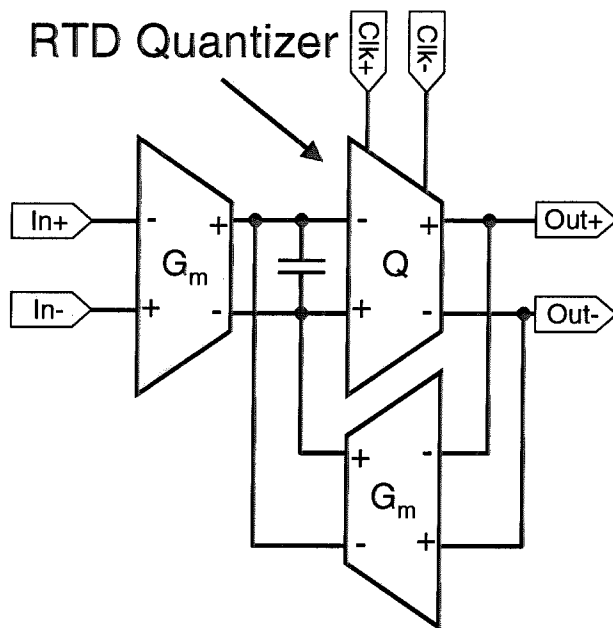


Figure 5. Schematic diagram of a continuous time first order Sigma-Delta modulator using the RTD-bridge quantizer. The quantizer can be as shown in Figures 1 through 4; with the quantizer in Figures 4 or 3 preferred for higher sampling-frequency operation.

shows a first order continuous-time current-steering implementation [10] ideally suited for the RTD-bridge quantizer. With the RTD-bridge quantizer the current-steering Sigma-Delta modulator in its simplest form then consists of 4 transconductance amplifiers, 1 RTD-bridge, and 1 capacitor.

The higher sampling rates enabled by the RTD-bridge quantizer allow the Sigma-Delta modulator to operate at higher oversampling ratios as compared to conventional FET-only designs, resulting in a higher number of effective bits at a given signal bandwidth.

5. Conclusion

In summary, new RTD based circuits for latched logic circuits, quantizers, and Sigma-Delta modulators capable of operating at 10 GHz and faster have been introduced. The RTD-bridge is an essential enabling component for the highest speed of operation. Through a minor circuit modification, RTD-bridge quantizers can be set up to operate in either a binary or a ternary mode. In addition, the use of an alternating clock across the

bridge enables the RTD to reset by discharging, eliminating the need for a FET-reset method. Also, since the RTD-bridge quantizes the input signal on each clock edge, a data sampling-rate of twice the clock frequency is obtained. This doubling of the sampling frequency is achieved *without* resorting to "ping-pong" operation of circuits and *without* incurring a component count penalty.

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