Fault Coverage Estimation for Early Stage of VLSI Design

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Abstract

This paper proposes a new fault coverage estimation model which can be used in the early stage of VLSI design. The fault coverage model is an exponentially decaying function with three parameters, which include the fault coverage upper bound, UB, the fault coverage lower bound, LB, and the rate of fault coverage change, α. The fault coverages using three different testing scenarios, which are no DFT, scan, iddq testing, are predicted using circuit design information, such as gate count, IO count, and FF count. These parameters are often readily available at the esrly stage of VLSI design. Finally, the composite fault coverage is estimated by combining different fault coverages. Experimental result showed a 1.9% model estimation error with a given circuit information in the early design.

1 INTRODUCTION

The advent in VLSI technology emphasizes a sophisticated chip design, mainly, manufacturable and testable design. One of the main concerns of the VLSI chip manufacturers is testing of a complex IC chip. Testing a complex IC without applying proper design for testability(DFT) methodology is almost impossible in practice. Therefore, many DFT techniques have been developed to increase the testability of a chip. Unfortunately, no DFT technology can guarantee a 100% testable chip, because the testability of a chip depends on the characteristics of the chip. As a result, it remains as a challenging task to estimate the testability of a chip regardless of the implemented DFT features.

Goel[1] developed several empirical models for estimating fault coverage. He proposed a two-phase testing strategy, the first is the initial test phase using random/pseudorandom test, and the second is the saturated test phase using deterministic test. He used a decaying exponential function to fit the phase one fault coverage and a linear function for the second phase. Savir et al.[2] proposed a random pattern testing to measure the testability of a chip using the signal probability estimation. Williams[3] and Huang et al.[4] predicted random pattern fault coverage with exponential functions, where the fault coverage is a function of the test length. Majumdar et al.[5][6] estimated the test length and fault coverage in random/pseudorandom testing using probability distribution function(pdf). Huisman[7] analyzed the reliability of several testability analysis programs [8][9][10][11][12][13]. Agrawal[14] assessed the effectiveness of the testability measures.

In this paper, we propose a new approach predicting the testability of a chip without detailed fault simulation. The testability of a chip can be estimated using fault coverage prediction model, which has been developed empirically. The proposed fault coverage model can apply for random combinational circuits as well as random sequential circuits.

2 FAULT COVERAGE MODEL

Previous work in the area of predicting the fault coverage of a chip showed the fault coverage is an exponentially decaying function[1][3]. Our bridge fault coverage simulation results of ISCAS 85 and 89 benchmark circuits are also well matched with the exponentially decaying function. We target bridge fault coverage because the bridge fault is more realistic to represent the faulty behavior of physical defect in CMOS technology. Ferguson et al.[15] revealed that a complete stuck-at fault test set can detect only a small portion of the total bridge faults. However, the number of bridge faults increases exponentially with increase in chip complexity, and hence it is often impractical to simulate all bridges. A random sampling approach has been used based on Acken's work[16][17].

The fault coverage depends on various characteris-

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tics of the chip, such as the gate count, the flip-flop count, and the IO pin count. Among them, The gate per io, G_{IO}, has been selected as the principle circuit parameter to estimate the fault coverage of a chip. The G_{IO} represents the difficulty of the chip being tested. If the G_{IO} value is large, which indicates the chip has a relatively deep logic depth. The internal nodes of the chip are difficult to control and to observe. Therefore, the chip is more likely to have a poor fault coverage. The gate per input, G_{IN}, can also be used to represent the controllability of a chip. In iddq testing, the testability depends on controllability, because the observability of the chip is guaranteed using the current monitoring. Therefore, G_{IN} can be used to estimated the iddq fault coverage of a chip. The feedback ratio, β, defined as the flip-flop count divided by flip-flop and IO count, can also be used to measure the sequentiality of a chip. It represents the relative sequential depth of a chip. The G_{IO}, G_{IN}, G_{FF}, and β are defined in Equation (1)-(3).

$$G_{IO} = \frac{gate}{in + out} \quad (1)$$

$$G_{IN} = \frac{gate}{in} \quad (2)$$

$$\beta = \frac{ff}{in + out + ff} \quad (3)$$

The proposed fault coverage estimation model is shown in Equation (4) and illustrated in Figure 1. Figure 1 shows the fault coverages of "Chip m" and "Chip n". Let LB be the fault coverage lower bound, which is the initial fault coverage, and UB be the fault coverage upper bound, which is the saturated fault coverage. Also, let α and A be the rate of increase for the test coverage measure, and the difference between LB and UB. Equation (4) shows that the fault coverage C is an exponentially decaying function with three parameters, UB, A, and α. The relationship between the lower bound LB and coefficient A is defined in Equation (5).

$$C = UB - A \times e^{-\alpha \times test} \quad (4)$$

$$LB = UB - A \quad (5)$$

$$C' = \alpha \times A \times e^{-\alpha \times TL} \leq C_{th} \quad (6)$$

$$TL = \left(-\frac{1}{\alpha}\right) ln \left(\frac{C_{th}}{\alpha A}\right) \quad (7)$$

Finding the optimum test length, TL, where the fault coverage is saturated, is important to measure the testability of a chip and to determine the optimum test length. The first derivative of fault coverage model, shown in Equation (6), represents the rate of change in fault coverage as a function of test length. The TL can

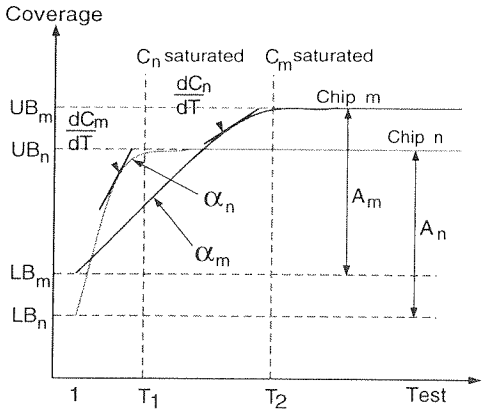


Figure 1. Two fault coverages

be found where $\frac{dC}{dtest}$ becomes just below a threshold value C_{th}. Equation (7) is obtained by solving Equation (6) for TL. In Figure 1, T_1 and T_2 denotes TL for "Chip m" and "Chip n", respectively.

The characteristics of ISCAS circuits are shown in Table 1. Figure 2 shows the simulation results of the selected circuits, in which the dots are the fault coverage measures, the solid line in the middle is the prediction by the model, and the two dotted lines are 95% confidence range of the fault coverage model.

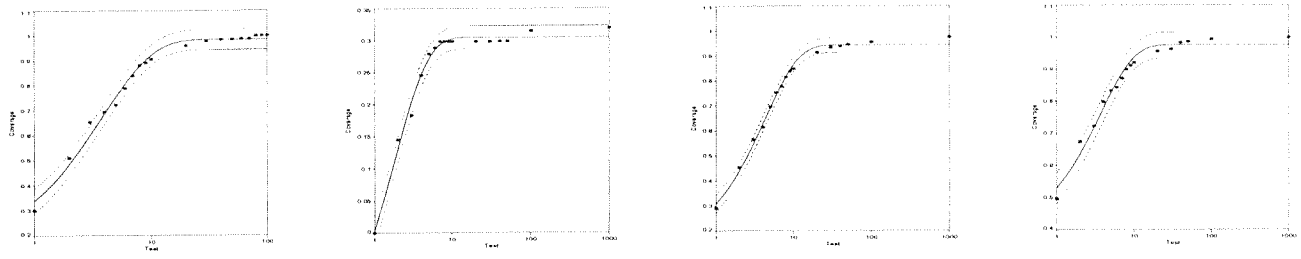
The process of building the models is such that one half of the benchmark circuits were selected for building the models through curve-fitting, and the other remaining half were used to verify the models. The curve-fitting process resulted in the following relationships among various model parameters shown in Equations (8)-(19). Table 2 summarizes the value of the coefficients in the above Equations. In the combinational model, UB, A, and α are all exponentially decaying function of G_{IO}. In the sequential model, the sequential feedback parameter β is introduced to incorporate the sequentiality of the circuit to estimate the fault coverage. For large β, UB, A, and α decrease rapidly with increase in G_{IO} value. In the full-scan model, the circuit becomes pure combinational circuit. As a result, the full-scan model does not contain β. In the iddq model, G_{IO} is substituted by G_{IN}. In the iddq testing, the observability is guranteed through steady-state current monitoring. Therefore, the controllability is the only measure for iddq testability. As a result, G_{IN}, which represents the controllability of the circuit, is used to estimate the iddq fault coverage instead of G_{IO}.

$$UB(comb) = exp[-c_0 - c_1 \cdot G_{IO}] \quad (8)$$

$$A(comb) = exp[-c_2 - c_3 \cdot G_{IO}] \quad (9)$$

$$\alpha(comb) = exp\left[-c_4 - c_5 \cdot \sqrt{G_{IO}}\right] \quad (10)$$

$$UB(seqn) = exp[-c_0 - c_1 \cdot \beta \cdot G_{IO}] \quad (11)$$



(a) C880 comb (b) S382 seqn (c) S713 scan (d) S1196 iddq

Figure 2. Fault simulation results

Table 1. ISCAS circuit information

	Gate	IO	FF	G_{IO}	β
C432	138	43	0	3.2093	
C499	180	73	0	2.4658	
C880	212	86	0	2.4651	
C1355	366	73	0	5.0137	
C1908	308	58	0	5.3103	
C2670	537	221	0	2.4299	
C3540	722	72	0	10.028	
C5315	1145	301	0	3.8040	
C6288	1848	64	0	28.875	
C7552	1474	313	0	4.7093	
S208	96	13	8	7.3846	0.3810
S298	119	9	14	13.222	0.6087
S344	160	20	15	8	0.4286
S349	161	20	15	8.05	0.4286
S382	158	9	21	17.556	0.7
S386	159	14	6	11.357	0.3
S400	164	9	21	18.222	0.7
S420	196	21	16	9.3333	0.4324
S444	181	9	21	20.111	0.7
S510	244	26	6	9.3846	0.1875
S526	193	9	21	21.444	0.7
S641	379	59	19	6.4237	0.2436
S713	393	58	19	6.7759	0.2468
S820	289	37	5	7.8108	0.1190
S832	287	37	5	7.7567	0.1190
S838	514	35	32	14.686	0.4776
S1196	529	28	18	18.893	0.3913
S1238	508	28	18	18.143	0.3913
S1423	657	22	74	29.864	0.7708
S1488	653	27	6	24.185	0.1818
S1494	647	27	6	23.963	0.1818
S5378	2779	84	179	33.083	0.6806

Table 2. Fault coverage model coefficients

Test	Coefficients					
	c_0	c_1	c_2	c_3	c_4	c_5
comb	0.030	0.004	0.176	0.004	0.838	0.403
seqn	0.120	0.029	0.038	0.033	1.000	
scan	0.070	0.008	0.079	0.020	0.429	
iddq	0.025	0.004	0.494	0.004	1.066	5.3e-7

$$A(seqn) = exp[-c_2 - c_3 \cdot \beta \cdot G_{IO}] \quad (12)$$

$$\alpha(seqn) = \frac{c_4}{\beta \cdot G_{IO}} \quad (13)$$

$$UB(scan) = exp[-c_0 - c_1 \cdot G_{IO}] \quad (14)$$

$$A(scan) = exp[-c_2 - c_3 \cdot G_{IO}] \quad (15)$$

$$\alpha(scan) = \frac{c_4}{G_{IO}} \quad (16)$$

$$UB(iddq) = exp[-c_0 - c_1 \cdot \beta \cdot G_{IN}] \quad (17)$$

$$A(iddq) = exp[-c_2 - c_3 \cdot \beta \cdot G_{IN}] \quad (18)$$

$$\alpha(iddq) = exp\left[-c_4 - c_5 \cdot \beta^3 \cdot G_{IN}^3\right] \quad (19)$$

Maxwell et al.[19][20] emphasized the importance of using a composite fault coverage metrics. It is common to test ICs using several testing strategies to ensure the quality. The way to derive the composite fault coverage measure, is not known. The fault coverage distribution of the applied test suite depends on the characteristics of a chip, and therefore it is difficult to generalize the relationship among different types of test. In our study, we assume that all faults are statistically independent. The composite fault coverage, C_{tot}, can be approximated using the following Equation.

$$C_{tot} = 1 - (1 - C_{no\ DFT}) \cdot (1 - C_{scan}) \cdot (1 - C_{iddq}) \quad (20)$$

The developed fault coverage models are evaluated using the remaining halves of benchmark circuits, which are never seen by the models. The estimation error showed about 3% error(combinational circuits) to 25% error(sequential circuits). The iddq estimation error showed large error, because the estimation error for the iddq testing has been evaluated at test length of 1, 5, and 10, instead of 10, 100, 1000 in other testing.

3 APPLICATION OF THE MODEL

A commercial VLSI ASIC device was used to validate the fault coverage estimation model. The random

Table 3. Chip fault coverage estimation result

Fault Coverage	Error compared with IC production data
scan Coverage	9.9%
iddq Coverage	13.1%
Composite Coverage	1.9%

logic part of the chip consists of 227,000 gates. The chip has been developed using standard cell design and manufactured using 0.5μm CMOS with four layers of metal interconnect. The chip size is about 105.8mm^2, and its operating voltage is 3.3V. It has 12477 fully scannable flop-flops and 58.7K-bit memory. The fault coverage estimation based on scan model showed a 9.9% estimation error, and iddq coverage showed a 13.1% estimation error. The composite fault coverage has been estimated using Equation (20). The model estimation showed about 1.9% error compared to the IC production data. Table 3 summarizes the fault coverage estimation result of the chip.

4 CONCLUSION

An early fault coverage estimation can help to prevent painful design modifications in the later design stages, and ensures quality manufacturing at lower cost. However, the fault coverage is usually unknown until the final stage of the design process. Therefore, it is sometimes unavoidable to revise the design due to the chip testing problems discovered in the later stage of the design. In order to solve this problem, we propose a new fault coverage estimation model, which can be used in the early design. The proposed model is a function of basic circuit design parameters, including the gate count, the input-output count, and the flip-flop count. Three different testing strategies, which include no DFT testing, scan testing, and iddq testing, are investigated to develop the fault coverage estimation model. The fault coverage estimation model is an exponentially decaying function with three parameters, the fault coverage upper bound, UB, the fault coverage lower bound, LB, and the rate of fault coverage increase, α. The model has been developed empirically based on the fault simulation results. A commercially developed ASIC chip was evaluated for validation purpose. The experimental result showed a good prediction accuracy as a first order approximation tool.

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