Novel Design for Testability of a Mixed-Signal VLSIC

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Abstract

A novel testability architecture has been developed for a mixed-signal VLSIC which has a functional architecture consisting of a microprocessor core, RF transceiver, and two voltage regulators. It permits a decoupling of analog/RF, digital, and power systems for individual stimulation and analysis. Testing may be performed at the subsystem or block level, and traditional scan techniques are augmented to allow mixed static and dynamic test. This approach aids in identifying any detrimental interaction between individual subsystems by providing isolation between the circuit-under-test and idle circuits.

1. Introduction

A major challenge in verification of mixed-signal VLSICs is real-time testing of analog and digital subsystems. Digital switch-level logic is amenable to exhaustive testing through standard scan techniques, but this approach is insufficient for dynamic analog circuits [1,2]. Also, scan techniques may fail to identify dynamic timing hazards which appear only during continuous operation. Although analog testing buses have been developed, they do not readily permit access to individual subsystems or do not sufficiently integrate surrounding digital logic [3]. This paper describes a novel testability architecture for a mixed-signal IC which emphasizes real-time testability. Under this architecture, the IC can be arbitrarily partitioned into analog/RF, digital, and power subsystems. Further decomposition can isolate circuits at the block level for fine-grained testing. This approach is valuable in identifying detrimental interaction between individual subsystems by providing isolation between the circuit-under-test and idle circuits.

2. Architecture

The functional architecture consists of a digital processor core, a 400-MHz RF transceiver, an I/O interface linking the processor to communications, and two on-chip dc-dc voltage converters for integrated power management. The digital core consists of an 8-bit 33-MHz CPU and a 256-byte SRAM for local program store and exercising the digital circuits. The zero-IF transceiver uses an ASK modulation of eight baseband tones in a 100-kHz bandwidth for digital communications. Baseband signal recovery is achieved with parallel envelope detectors (FVC) which translate the ASK modulation into a binary word. The output of eight parallel ring-oscillators (VFC) is gated with a binary word to generate the ASK-modulated baseband signal. Communication with the digital core is also possible through unidirectional 8-bit buses routed to the IC pins. Die orientation is shown in Fig. 1 and pin assignments are listed in Table I. The RF I/O state machine is described in Fig. 2.

2. Testability

2.1. Digital Subsystem

Core digital functional testability is provided by a 152-bit FIFO serial scan path (SCANIN to SCANOUT) controlled by an enable pin and a clock (SCANEN and SCANCLK) joining all internal data registers, address registers, and state-machine variables, including all interrupt flags. The complete controllability and observability of the scan path guarantees full static testability of the sequential logic. Only partial test of state machines is possible since not all SM inputs are available to the scan path; however, since the internal state

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variables are visible, the state activity can be monitored and adjusted during dynamic testing. By decoupling the scan clock and operating clock, scan data can be inserted and reviewed at any time during continuous operation.

2.2. Analog/RF Subsystem

The mixed-signal testability architecture consists of a switch matrix embedded within the functional VLSI architecture (see Fig. 3). Multi-purpose internal buses serve dual roles for testability and continuous circuit operation. Partitioning of the systems for test is defined by external control of IC pins (viz. TESTC1, TESTC2, TESTC3, and TESTM) which configure the internal switch matrix. Table II lists the possible test configurations and pin settings. In the various dynamic test modes, the transceiver can be tapped at several locations: (in the receiver) before and after the down-mixer and prior to baseband signal recovery, and (in the transmitter) after baseband signal generation and after the up-mixer. Pins TESTC1, TESTC2, and TESTC3 can be ganged together or applied individually.

A multi-purpose internal bus can either perform according to its functional specification or provide a stimulus/response path to IC pins. Reuse of internal buses reduces layout dimensions by eliminating dedicated test routing, and it allows measurement of bus characteristics by injecting signals or monitoring bus outputs. For RF test, RFMUX can be set high or low. In standard (test) mode data "received" by RF I/O is provided by the FVC (external bus). Data sent for RF transmission is always mirrored to a second external bus. External buses can be used for test or sent to an external bus controller (e.g. I2C) for wired communication.

2.3. Mixed-Mode Testability

In mixed dynamic and static test, real-time execution can be halted to view or edit internal elements of the scan path; following the scan operations real-time execution is resumed. This technique of breakpointing can verify that internal states have responded correctly to dynamic events. Logic states can also be preset statically through the scan path to artificially induce desired responses upon return to continuous test. Mixed-mode testing can be used to verify operation of interrupt handling between the CPU and the memory or RF/I/O subsystems.

2.4. Power Management Subsystem

Testing of the two dc-dc voltage converters can be done independently of normal operation. Each converter outputs its regulated voltage level to an external pin (viz. DCOUTA or DCOUTD), shown in Fig. 4. Connection to internal circuitry is enabled by connecting a jumper between the regulated output and the corresponding input (e.g. DCOUTA to VDDA). External linkage also allows a performance comparison between operating using the internally regulated supply and a stable external supply.

3. Physical Design and Fabrication

The mixed-signal VLSIC and testability architecture has been implemented on the 0.25-micron fully-depleted (FD) SOI CMOS process of MIT/Lincoln Laboratory and is currently undergoing fabrication. Intended primarily for ultra-low-power digital logic, employing supply voltages of less than 2 V, the MIT/LL FDSOI process is not well characterized for analog and high-frequency (RF) performance. This architecture will help identify signal integrity troubles.

4. Conclusions

A mixed-signal testability architecture has been designed and implemented for flexible functional test and identification of signal integrity hazards. These effects are more significant at extremely low voltage levels as undesirable noise can achieve a magnitude which is a large percentage of the supply voltage. The testability architecture we have developed is essential for verification and characterization of this and future low-power mixed-signal VLSICs, and is part of our ongoing work into system-on-a-chip ICs [4].

5. Acknowledgment

This work was in part performed at the Center for Integrated Space Microsystems, Jet Propulsion Laboratory, California Institute of Technology. This was sponsored by the National Aeronautics and Space Administration.

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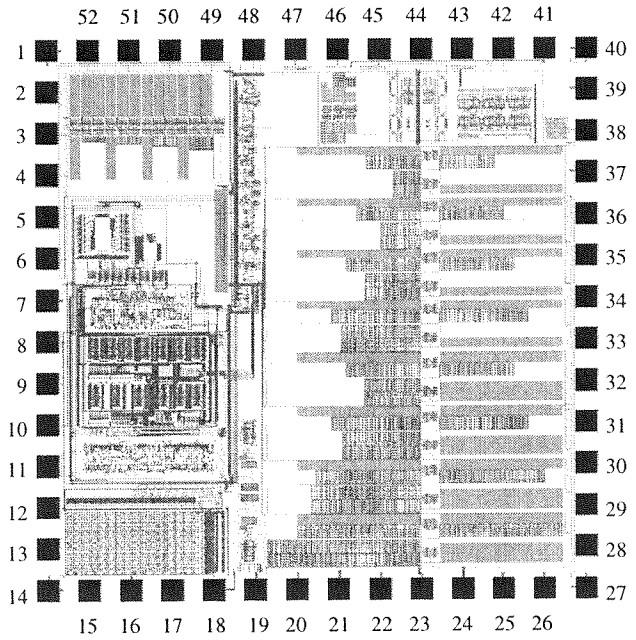

Fig. 1 Die orientation and pin labeling.

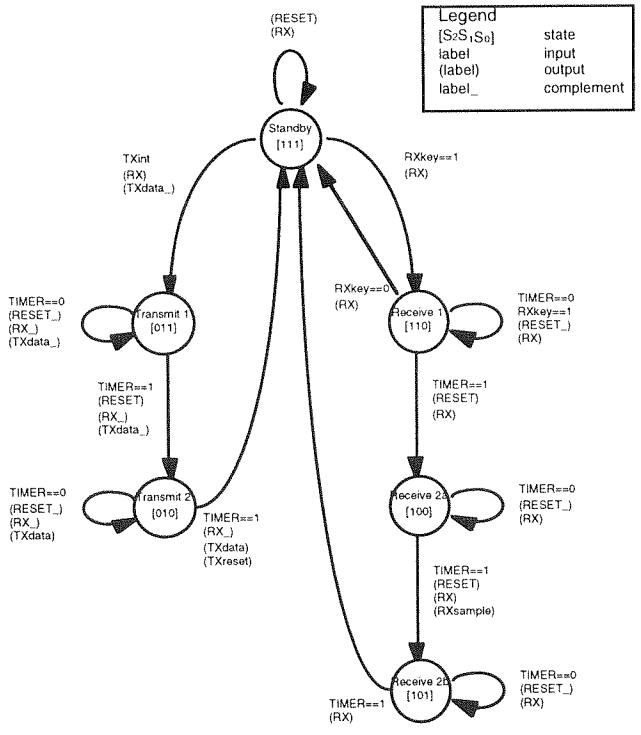

Fig. 2 RF I/O state machine.

Table I Pin assignments.

Pin	Abbreviation	Function	Direction
1	GNDD	digital ground	I
2	TESTC1	AD/DA converter test pin	I
3	IBUS<3>	input bus <3>	I
4	IBUS<2>	input bus <2>	I
5	IBUS<1>	input bus <1>	I
6	IBUS<0>	input bus <0>	I
7	SHIELD1	shield ground #1	I
8	RESET_	system reset	I
9	CLOCK	clock	I
10	SCANIN	scan chain input	I
11	SCANEN	scan chain enable	I
12	SCANCLK	scan chain clock	I
13	SCANOUT	scan chain output	O
14	GNDD	digital ground	I
15	NC	no connection	Z
16	SHIELD2	shield ground #2	I
17	VDDD	supply rail (digital)	I
18	DCOUTD	dc-dc converter (digital)	O
19	BATTERY	battery input (2 V)	I
20	DCOUTA	dc-dc converter (analog)	O
21	VDDA	supply rail (analog)	I
22	SHIELD3	shield ground #3	I
23	VREF	reference voltage	I
24	VBIAS	bias voltage	I
25	NC	no connection	Z
26	NC	no connection	Z
27	GNDD	digital ground	I
28	OBUS<0>	output bus <0>	O
29	OBUS<1>	output bus <1>	O
30	OBUS<2>	output bus <2>	O
31	OBUS<3>	output bus <3>	O
32	TESTC2	AD/DA converter test pin	I
33	OBUS<4>	output bus <4>	O
34	OBUS<5>	output bus <5>	O
35	OBUS<6>	output bus <6>	O
36	OBUS<7>	output bus <7>	O
37	SHIELD4	shield ground #4	I
38	ANTENNA	RF antenna	IO
39	SHIELD5	shield ground #5	I
40	GNDA	analog ground	I
41	TESTC3	AD/DA converter test pin	I
42	TESTM	mixer test pin	I
43	DMIXI	down mixer test input	I
44	LO	local oscillator	I
45	UMIXI	up mixer test input	I
46	VFCO	VFC test output	O
47	FVCI	FVC test input	I
48	RFMUX	bus select pin	I
49	IBUS<7>	input bus <7>	I
50	IBUS<6>	input bus <6>	I
51	IBUS<5>	input bus <5>	I
52	IBUS<4>	input bus <4>	I

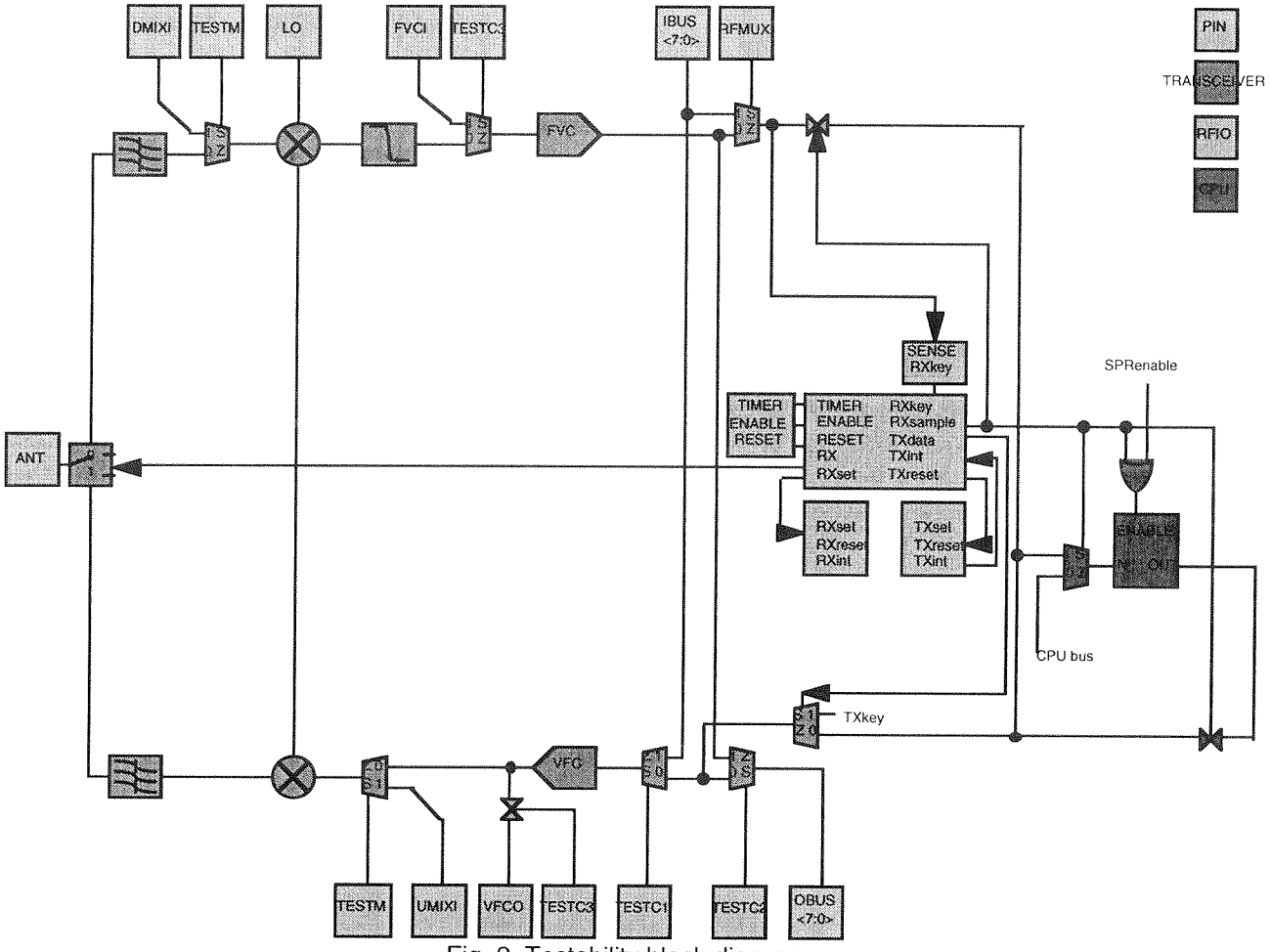

Fig. 3 Testability block diagram.

Table II RF/analog test pin settings and configurations.

Function #	RFMUX	TESTC(1-3)	TESTM	Operation
1	don't care	0	0	• Normal system operation
2	don't care	0	1	• Test DMIX: apply input to DMIXI with no output detection • Test UMIX: apply input to UMIXI and detect output at antenna (Note: must also set antenna direction to output by scan path.)
3	don't care	1	0	• Test FVC: apply input to FVCI and detect output at OBUS<7:0> • Test VFC: apply input to IBUS<7:0> and detect output at VFCO
4	don't care	1	1	• Test UMIX: apply input to UMIXI and detect output at antenna (Note: must also set antenna direction to output by scan path.) • Test FVC: apply input to FVCI and detect output at OBUS<7:0> • Test VFC: apply input to IBUS<7:0> and detect output at VFCO

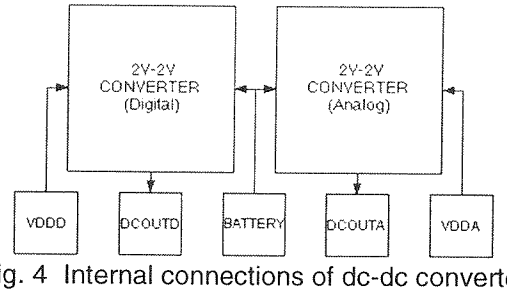

Fig. 4 Internal connections of dc-dc converters.