On Optimizing Test Strategies for Analog Cells

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Abstract - *The purpose of this paper is to analyze an optimization method to improve the testability of structural defects, such as bridges and opens, in low-power low-voltage analog circuits. The approach consists of finding an optimum subset of tests which maximizes the fault coverage with minimum cost. An application example is given to illustrate the proposal by studying the fault coverage obtained using different test sets on a simple 2-stage Nested Transconductance Capacitance Compensated (NGCC) amplifier.*

1 Introduction

Defect characterization in analog circuits is an important task and a desirable approach for producing testable complex systems. The size and densities of analog circuits continue to increase but the detection and isolation of faults in these circuits becomes more difficult due to the nature of analog faults.

The usual practice in analog and mixed-signal testing is based in verification of the functionality of the circuit by verification of some "representative" design specifications. This approach widely used at present, known as *functional testing*, may produce a large number of escapes (circuits with defects which pass all the specs tested). In addition, some parts of the circuit become over-tested because some tests are redundant and could be eliminated.

An alternate approach very successful in the digital domain is based in targeting the set of possible defects of the IC. In this work we are focusing our attention in trying to find optimum test sets for small analog cells with physical defects which are known to occur with high probability in the fabrication process. The *structural testing* approach is harder in the analog world due to the fact that the characterization of the defective behavior is significantly more complex than in the digital world. To overcome these difficulties we are modeling the defects in a way that is treatable and we are making a few simplifying hypothesis which will be used in the evaluation of the defect coverage of each set of tests. It is clear that the computational effort may grow considerably and we will target small cells to be able to guarantee the applicability of the optimization method proposed. For larger circuits a hybrid *functional/structural* approach is currently under investigation.

In this paper, an optimization method to improve the testability of structural defects in low-power low-voltage analog circuits is proposed. The approach consists of finding an optimum subset of tests which maximizes the fault coverage with minimum cost. The rest of the paper is organized as follows: section 2 proposes the optimization method when testing structural defects, such as bridges and opens. The test strategies (Quiescent and Transient) applied are described in section 3, together with the results obtained in the analog cell used to illustrate this method. Section 4 summarizes and presents the conclusions.

2 Optimization Method

Given a set of tests applied to an analog circuit to detect structural defects, each of them varying in a continuous range, the main objective of the proposed method will be to find a subset of tests which allows the maximum fault coverage with minimum cost. In order to simplify the selection of the optimum test set, the following hypothesis are accepted:

- H1 The list of "possible" defects is available. This final list of candidates for defects (*catastrophic* or *parametric*) is obtained by Inductive Fault Analysis and by information supplied by the process engineers on likely defects of the fabrication technology used to fabricate the CUT.
- H2 Each defect, *catastrophic* or *parametric*, is modeled by a set of ranges in its model parame-

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ters. For instance, the resistances of the bridging defects are assumed to belong to the interval $[0, 20k\Omega]$ [1].

H3 The values of the defect parameters are assumed equally likely in the range of variations, and the non defective CUT parameters are assumed to take the *nominal* value of its specification.

H4 A set of n analog tests $\{T_i$, i=1..n$\}$ is available and the cost to perform each test is known $\{w_j$, j=1..n$\}$. These tests cover all *non redundant* defects.

2.1 Resistive bridges

Let us apply n different test methods (T_i, i=1..n) to m possible resistive bridges (R_j, j=1..m), with values in the above mentioned interval. Assume that test T_i detects a sub-range of R_{Bi} values, which can be different from those detected from another test, T_k ($i \neq k$, as is shown in figure 1). The *continuous cover* of T_i *versus* R_j can be translated into binary values (see figure 2) if the R_B range is partitioned into discrete sub-ranges. This is achieved taking into account that a '1' represents a completely shaded interval, being '0' otherwise. Therefore, the binary *sub-range coverage* matrix can be written, as follows:

$$C_B(T_1, T_2, ...T_n) = \begin{pmatrix} 1 & 0 & 0 & 0 & \dots & 0 & 0 \\ 0 & 1 & 0 & 0 & \dots & 1 & 1 \\ 1 & 0 & 0 & 0 & \dots & 1 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 1 & 1 & 0 & \dots & 1 & 0 \end{pmatrix}$$

2.2 Floating-gate Defects

The analysis of the floating-gate case is more complex, because we do not deal with a one-dimensional problem. As developed in the digital domain [2] and extended to the analog domain [3], the floating gate defect is characterized at the electrical circuit level, taking into account the technology and topology of the circuit, and the physical location of the break. For a given circuit topology, the FG defect parameters can be fully represented by: A) the length of the poly line from the open to the transistor's gate, L_{BREAK}, and B) the intrinsic charge, Q'_0 [4].

Once the layout has been drawn and the parasitic coupling capacitances extracted, the regions of detectability can be found as two-dimensional functions (L_{BREAK} *versus* Q'_0), depending on the test applied, as depicted in figure 3a. These regions are splitted into *areas* of detectability (see figure 3b). In order to translate this problem into a one-dimensional situation, every region can be partitioned in *detectable sub-regions*.

Let us assume m different regions, A_j, j=1..m as a result of n different tests applied, T_i, i=1..n. If region A_j is detected by tests T_i and T_k ($i \neq k$), then it can be written as the detectability sub-region vector $C_{0..010..010..0}$ (see figure 4), where the '1s' indicate the positions corresponding to tests T_i and T_k, respectively. The conversion into a matrix form is automatic, as shown as follows:

$$C_{FG}(T_1, T_2, ...Tn) = \begin{pmatrix} 1 & 1 & 0 & \dots & 1 \\ 0 & 0 & 0 & \dots & 0 \\ 0 & 0 & 0 & \dots & 0 \\ 0 & 1 & 1 & \dots & 0 \\ \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & 1 \end{pmatrix}$$

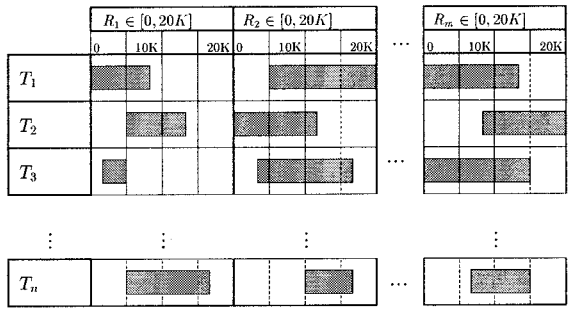

Figure 1 FCs for bridges, partitioned into *sub-ranges*.

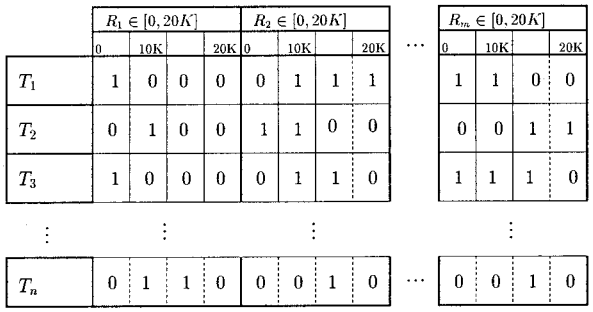

Figure 2 Translation of continuous ranges into binary values.

2.3 Direct-path opens

The matrix for the direct-path open is directly written, because there are no ranges nor areas of coverage. The D-P open is detected ('1') or not detected ('0').

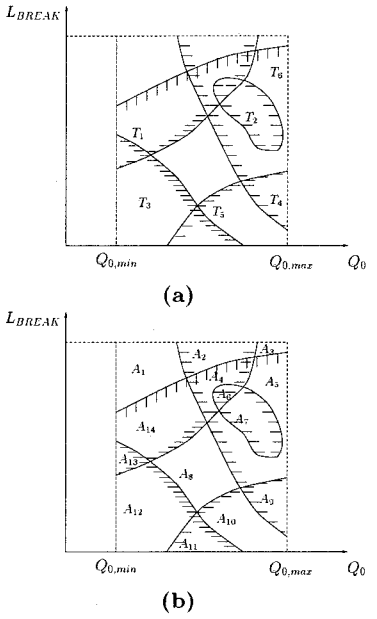

Figure 3 (a) FCs for different test methods used to detect FGDs. (b) Partitioning into *regions*.

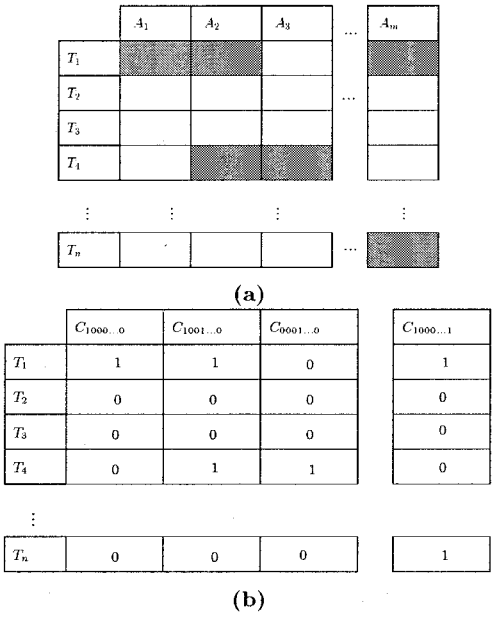

Figure 4 Translation of (a) continuous regions into (b) a partition of sub-regions (and thus, into binary values).

2.4 Goals

Once the matrices have been built, it is important to give *weights* (w_{Tj}, j=1..n) to the rows, depending on the application effort of the test method; *i.e.*, the more complex the highest weight. Keeping in mind that the essential columns (that is, those columns with only one '1') have to be compulsory considered, the main goal will be to find the **test set** which covers all defect regions, with minimum cost ($T_{sel-set}$). The previous sentence can be mathematically expressed as:

$$\left.\begin{array}{ll} Cost & = min\left[\sum_{T_j \in T_{sel-set}} w_{T_j}\right] \\ \{T_{sel-set}\} & cover\ all\ defect\ regions \end{array}\right\}$$

For a general case, our final goal is equivalent to an optimal covering problem. Consequently, the final test set which covers the maximum regions will be obtained, taking into account minimum cost restrictions.

3 Results on the 2-NGCC

3.1 Test strategies

For testing complex analog systems, a circuit partitioning is done, and each sub-block is tested separately. Before testing begins, the test effort has to be quantified and various test options should be evaluated in order to minimize cost and maximize confidence. For the 2-stage NGCC amplifier [5] shown in figure 5, two test options have been considered:

1) Quiescent test, where the observables are the quiescent current (I_{DD}, I_{SSQ}) and the output voltage (V_{OUT}).
2) Transient test: (A) In *frequency domain*, where the low-frequency gain (A_o), the unity-gain bandwidth (GB), and the phase margin (Φ_m) are observed; (B) in *time domain*, where a $1\mu s - t_{rise}$ step has been applied to the circuit and the delay time has been measured.

For the 2-stage NGCC op-amp, the following selection criterion has been taken into account, in order to decide whether a fault is detected or not: a fault is detected if the error is greater than 5% in measuring I_{DD}, I_{SSQ}, V_{OUT}, GB and t_d, when error measures in A_o exceed 5 dB, and 5° when Φ_m is observed.

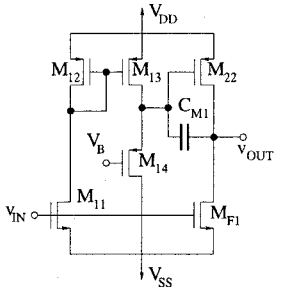

Figure 5 NGCC Amplifier Topology

3.2 Resistive bridges

Once the layout has been drawn, an IFA method has been used to find the resistive bridges (R_B) with a higher probability of occurrence: 11 of a total # of 21 (node-to-node) have been selected. Identifying the set of tests $\{T_1, T_2, T_3, T_4, T_5, T_6, T7\}$ as $\{I_{DDQ}, I_{SSQ}, V_{OUT}, A_o, GB, \Phi_m, t_d\}$, respectively, figure 6 depicts the regions of detectability for every kind of tests and for every bridge. As the selected circuit is sufficiently small to simplify the illustration of the method proposed, it is possible to make a visual selection of the optimum subset of tests which allows the maximum detectability (see figure 6). Effectively, a 100% of fault coverage (if only bridges were present) can be achieved when using tests T_2 (critical cases for R_{B2} and R_{B8} indicates that the I_{SSQ} test should be compulsory considered) and whatever of T_4, T_5 or T_6, which in turn correspond to A_o, GB and Φ_m, respectively. Both GB and Φ_m tests require the use of sophisticate measurement techniques which will increase the cost of test. Keeping this in mind, we conclude that the subset $\{T_2, T_4\}$ will provide the maximum coverage with minimum cost when detecting bridges in the 2-NGCC amplifier.

3.3 Floating-gate defects

Six floating-gate defects (corresponding to the six transistors of the circuit under test) have been analyzed. The floating-gate defects have been modeled according to the model proposed in [2] [3]. The poly-bulk capacitance, C_{pb} (capacitance poly-well, C_{pw} for the PMOS transistors) depends on the length of the poly path that goes from the gate to the location of the break, L_{BREAK}, as well as on the gate-substrate overlap capacitance [2]. On the other hand, taking into account the law of charge conservation in the gate node of a transistor with a floating-gate defect, it can be easily shown that the voltage induced at the gate, V_{FG} is straightforward proportional to the effective interface charge [4]. Therefore, the simulations have been done taking into account variations on L_{BREAK} and on Q'_0, whose regions of detectability are depicted in figure 7. As explained in section 2, these regions of detectability can be translated into detectable sub-regions, and thus into binary values (see figure 8). If only FGDs were considered, a 92% of fault coverage would be obtained when using test T_5, followed by T_4 and T_6 (87.5% FC), which correspond to GB, A_0 and Φ_m, respectively. Furthermore, T_7 (t_d) must be considered, because it is the only test which detects A_{13}. Although test T_5 provides the maximum FC, it is difficult to apply. Thus, there is a trade-off FC *versus* cost. The subset $\{T_4, T_7\}$ will be then selected as providing the maximum coverage with minimum cost.

3.4 General results

The fault coverage is the percentage of faults that are covered by a test set. In order to present a general result, the Circuit Under Test must be analyzed considering the partial results in the presence of all kinds of defects. For the case discussed in this paper, the final subset of tests which allows a 100% of fault coverage must consider those tests which optimally cover the defects. Effectively, taking into account the results obtained in sections 3.2 and 3.3, it can be concluded that a 98% of fault coverage will be obtained when using the optimum sub-set of tests, which is

$$\{T_2, T_4, T_7\}^* = \{I_{SSQ}, A_o, t_d\}$$

For larger circuits a hybrid *functional/structural* approach is currently under investigation.

4 Conclusions

An optimization method to improve the testability of catastrophic defects in low-power low-voltage analog circuits has been proposed. The approach consists of finding an optimum subset of tests which maximizes the fault coverage with minimum cost. Several test strategies have been analyzed for a low-power/low-voltage analog circuit. An accurate analysis has been performed in order to show the evolution of catastrophic defects (resistive bridges and floating-gates). The main parameters of the targeted cell have been tested for fault coverage in two domains (Quiescent and Transient) and the conclusions extracted.

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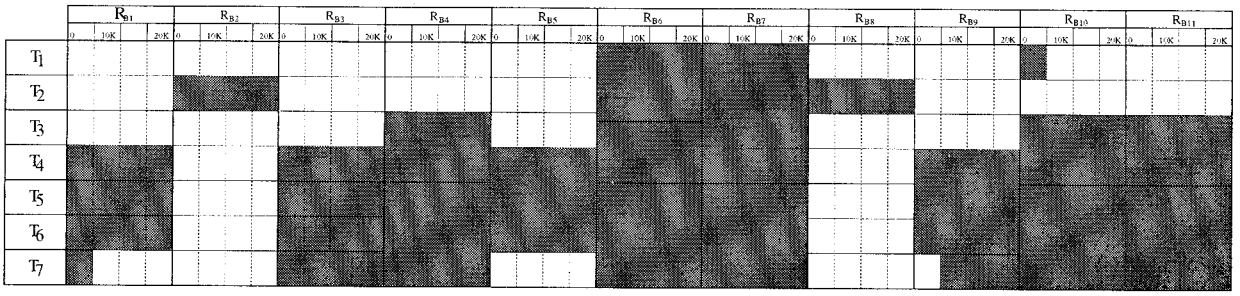
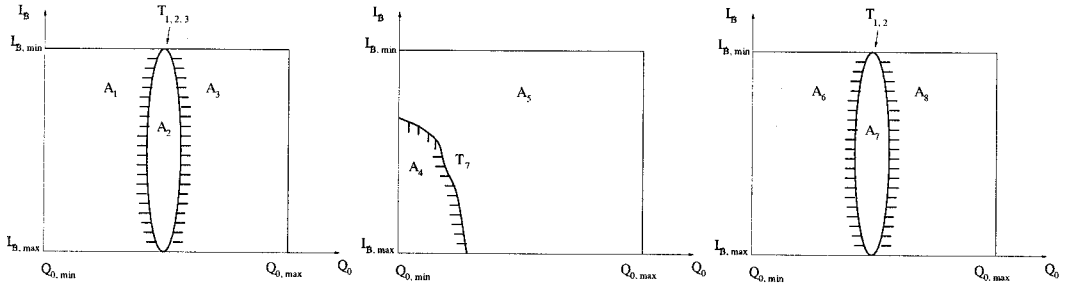


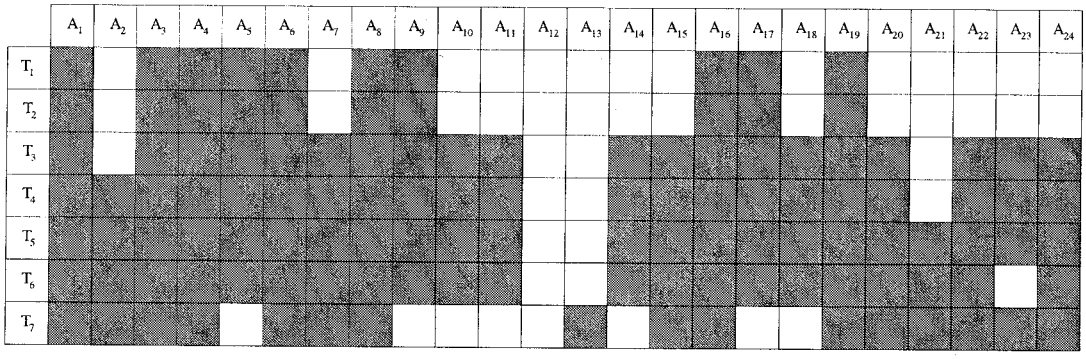
Figure 6 Regions of detectability for the bridges with a highest probability of occurrence in the 2-NGCC amplifier.



(a) FGD at M_{11} (double). (b) FGD at M_{12}. (c) FGD at M_{13}.

(d) FGD at M_{14}. (e) FGD at M_{22}. (f) FGD at M_{F1}.

Figure 7 Regions of detectability for the floating-gate defects in the 2-NGCC amplifier. According to [4], $Q'_{0,min} = 0.032fC/\mu m^2$ (minimum voltage induced at the gate, V_{FG}), $Q'_{0,max} = 0.16fC/\mu m^2$ (maximum V_{FG}). $L_{B,max}$ simulated for C_{pb}(C_{pw} for PMOS)= $1fF$ and $C_{pvdd} = 1fF$, while $L_{B,min}$ for $C_{pb} = 1fF$ and $C_{pvdd} = 10fF$.



$C_{1111111} = \{A_1, A_3, A_4, A_6, A_8, A_{16}, A_{19}\}$, $C_{1111110} = \{A_5, A_9, A_{17}\}$, $C_{0011111} = \{A_7, A_{15}, A_{20}, A_{22}, A_{24}\}$, $C_{0011110} = \{A_{10}, A_{11}, A_{14}, A_{18}\}$, $C_{0011101} = \{A_{23}\}$, $C_{0001111} = \{A_2\}$, $C_{0000111} = \{A_{21}\}$, $C_{0000001} = \{A_{13}\}$, $C_{0000000} = \{A_{12}\}$.

Figure 8 Regions of detectability for the FGDs in the CUT and translation into detectable sub-regions.

$\{T_1, T_2, T_3, T_4, T_5, T_6, T7\}$=$\{I_{DDQ}, I_{SSQ}, V_{OUT}, A_o, GB, \Phi_m, t_d\}$, respectively,