New 2 Gbit/s CMOS I/O pads

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Abstract

A couple of low complexity high performance input and output pads are proposed: they have been designed in 0.7 μm CMOS ES2 technology and support bit rates ranging from DC up to 2 Gbit/s. The differential input pad and the differential output pad interface true PECL external logic levels to full swing 5V CMOS internal levels.

1. Introduction

Current sub-micron technologies are able to support high speed clock frequencies also with standard static CMOS libraries; clock frequencies of the order of hundreds MHz can be achieved adopting new high speed dynamic families [1, 2, 3]. These solutions make possible the low cost implementation of chip cores with very high performance for several applications, ranging from microprocessors to real time dedicated DSP. Particularly interesting is the possibility of implementing high speed ASICs with standard CMOS technologies. However, standard CMOS I/O pads are limited to about 200 Mbit/s even due to power dissipation and power supply noise limitations. Therefore, serial to parallel conversion is required, so increasing the pin count and the power requirements. Higher speeds can be obtained through current mode topologies, which couple logic levels to currents rather than voltages [4, 5].

Two new pads for very high speed applications are described in this paper: an input differential pad and an output differential one. The described pads have been developed to meet the following constraints: maximum working frequency of 1 GHz with no lower bound (DC levels allowed), true PECL levels outside the chip, full swing 5V CMOS levels internally, external differential signals (to improve both speed and EMC), latchup and ESD protections, 0.7 μm ES2 CMOS technology. Besides it is assumed that the impedance matching to external input and output lines was accomplished outside the chip.

2. Input pad

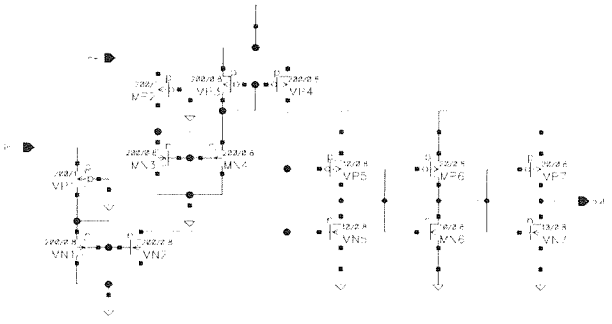

Figure 1. Input pad

The input pad schematic is shown in figure 1, where `in+` and `in-` are the differential PECL inputs and `out` is the CMOS internal signal. Each input signal directly feeds a p-channel MOS in a common gate configuration, as it is usually done for impedance matching to the external line. However, in this scheme the input device is not dimensioned to obtain this goal; instead it is inserted according to the following considerations:

- First of all, the use of a common gate configuration allows to obtain reasonably high speeds even with transistor length greater than the minimum one. This is a key point as, due to ESD and latchup considerations, some technologies require the use of longer channel devices for direct connections to input and output signals. From this point of view the input p-channel MOS allows the use of minimum length, faster devices in the ground referenced current mirrors, while guaranteeing higher immunity to latchup and ESD.

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- The input capacitance of the p-channel MOS is in parallel to the bonding pad one. So, it does not appreciably slow down input signal transitions whenever source capacitance is maintained negligible with respect to the bonding area one. This is another point to consider if internal impedance matching is chosen.

- The input current must flow through the bonding and package wire inductance. Using internal impedance matching will cause large current variations during signal transitions, i.e., larger voltage drop on the parasitic inductance. On the other hand, the input current cannot be too small, as it is exactly the current which will be used to swing the current mirror output voltage.

- The input device cannot be too small, as this will lead to a high voltage drop across it, leaving a reduced voltage swing to drive the weak side of the following current mirror.

The choice to have equal widths for the p-channel and the weak side of the current mirror seemed to be the best compromise.

The two received signals are then subtracted through current mirrors and the difference signal, represented by a current, is used to charge or discharge the input capacitance of a chain of three static inverters. The three current mirrors have a 1:1 mirror ratio, as strong side current transitions are as faster as the mirror ratio is reduced, while, on the other hand, capacitance driving capabilities of a current mirror depend strongly on output transistors dimensions.

The inverter chain at the output is used as a three stage voltage amplifier. In fact, due to the use current mirrors, the voltage swing at the input of the first inverter (at high switching speed) is reduced between approximately V_{Tn} and $V_{DD}-V_{Tp}$. The three inverters are then sized with the aim of reaching the full CMOS swing on the specified output load, while satisfying pad speed constraints.

Due to the high input currents required, the standard CMOS input protection obtained with the use of a series polysilicon resistance in the range of thousands of Ohm's cannot be used. On the other hand, the common gate input topology helps to obtain a better intrinsic ESD protection. Anyway, foldback MOS protections have been included in the design and their effects on circuit performance have been evaluated during electrical simulations of the layout. An avalanche topology has been used, to reduce the required width of protection devices, i.e. their capacitance loading of input signals.

3. Output pad

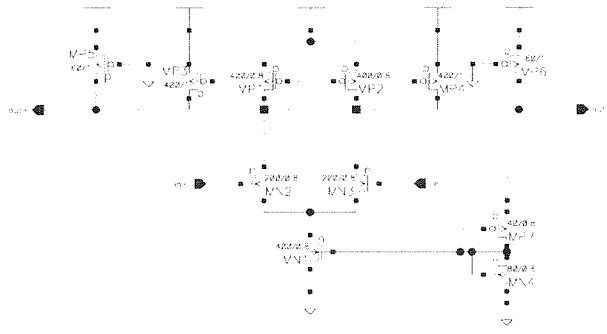

Figure 2. Output pad

The structure of the output buffer is given in figure 2, where `in+` and `in-` are the internal differential CMOS signals, while `out+` and `out-` are the PECL outputs.

The CMOS inputs are directly connected to a couple of n-channel devices, connected as a differential stage. Transistor MN1 is connected between the common source of the differential pair and ground, so acting as a standard current generator. Its gate voltage is obtained through a voltage splitter (MN4, MP7), and it's at a value suitable to guarantee saturation of MN1 in normal operating conditions.

However, these considerations are valid only for steady state or low speed operations. Otherwise, a more detailed analysis must be carried out. Applying full swing, fast transitions to the inputs (in the order of hundredth's of picoseconds) the differential pair can be best modeled as a simple current switch, where the 'on' transistor is just a little value resistance, while the 'off' one is really an open switch. The drain current switching occurs in a little region of the input voltage range, leading to a certain decoupling of the output slew rate from the input one. During input transitions, the current generator MN1 changes appreciably its behaviour due to its parasitic capacitances, which have a positive effect on transition speed, In fact, its gate to drain capacitance introduces a voltage feedback on the drain itself, which on turn increases the drain current of MN1 during transitions, so accelerating the fall of the drain voltage of the differential pair transistor which is turning on. This effect can be increased with a larger MN1 with respect to the size of the differential pair transistors, but, on the other hand, it cannot be too great, to have a reasonable drain to source voltage, sufficient to guarantee saturation in steady state conditions. The size of the voltage splitter built up by MP7 and MN4 has a great impact on the dynamic behaviour of MN1,

too, as its output capacitance reduces the amount of voltage feedback applied from the drain to the gate of MN1. These effects have been extensively analyzed through HSpice simulations of the circuit itself.

The current which flows through the 'on' branch of the input differential pair is then sent to the weak side of a current mirror, and it is replicated towards the corresponding output. This way, every time there will be a well determined current sourced by an output pin, while the complementary one will be disconnected. It will lead to a 'high' logic level corresponding to the power supply voltage. To achieve the specified PECL logic levels, two bleeder p-channel devices (MP5 and MP6) have been introduced, guaranteeing a maximum output voltage of 4.1V.

Even the two output current mirrors have been dimensioned analyzing the behaviour of the circuit during switching. The slew rate of the voltage output is different during falling and rising transitions. In fact, the rise of the output voltage is actively driven by the current which flows through the related current mirror, i.e. it depends on the current sunk by the differential pair branch currently 'on' and on the mirror ratio. On the other hand, the fall of the output voltage is driven by the external termination resistance, against the residual current which is flowing through the current mirror which is turning off. But the turn off of the current mirror is a self driven event. In fact, the turn off time of the differential pair transistor is much faster than the current mirror one. So, the only way to discharge the gate to source capacitance of MP1 and MP3 (or MP2 and MP4 for the complementary output) is through MP1 itself. It means, as already stated for the input pads, that the best turn off speed will be obtained with a reduced mirror ratio. These considerations, joint to the need to obtain reasonable transistor sizes and light loading of the internal CMOS driver, lead to the choice of a 1:1 mirror ratio.

The fully symmetrical structure of the output pad allows, if a balanced load is used, a strong reduction of EMI, as from the point of view of power supply noise as from the point of view of noise directly generated by the output signals. In fact, HSpice simulations have shown that the power supply current is fairly constant during a whole period of the output signals.

Latchup and ESD protections have been included in the design of the output pad, using same topology and devices used for the input pads.

4. Results and future works

The described pad structures have been synthesized using the ES2 0.7 μm CMOS technology, but different approaches have been used for the different part of the design. The layout of the input pad logic (represented in the schematic of figure1) has been obtained through the use of a standard cell layout synthesizer. Then this block has been inserted in a hand designed cell, including bonding pads and ESD/latchup protection devices. Figure 3 shows the obtained layout for the input pad.

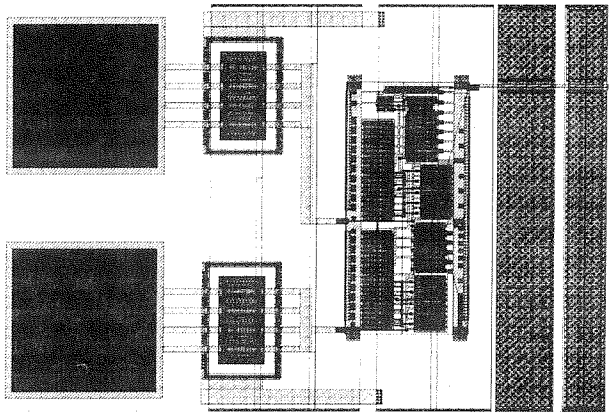

Figure 3. Layout of the input pad.

The layout of the output pad has been instead designed entirely by hand, due to the need of guard rings properly positioned around the devices connected to the output signals, and due to the high current levels used inside the circuit itself, which make impractical the use of an automatic router without incurring in electromigration problems. Moreover, a careful layout has shown the ability to strongly reduce the effect of interconnection capacitances and resistances on overall circuit speed. Figure 4 shows the obtained layout for the output pad.

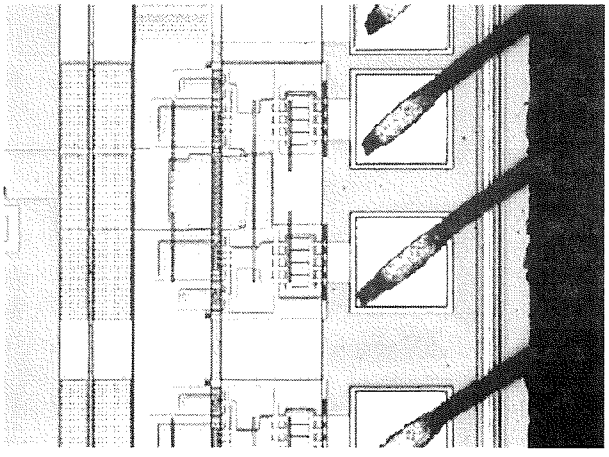

Figure 4. Microphotography of the output pad.

The two layouts have been designed to have the same pitch and power ring structure of the standard ES2 pads, so that they can be successfully used in integrated circuits with mixed high speed PECL compatible and CMOS low speed pins.

The occupied active area is 14,000 μm^2 for the input pad and 30,000 μm^2 for the output one, even if the actual area is quite larger due to the geometric constraints described above.

Post layout simulations have been performed for both pads, in order to verify the effects of protections and parasitic devices: an example of the results obtained using the HSpice models is given in figure 5, where the upper waveforms are the differential outputs for a 1 GHz signal, while the lower waveforms are related to the input pad simulations. In both simulations, the effect of source impedances as well as estimated bonding wire and package frame parasitics are included.

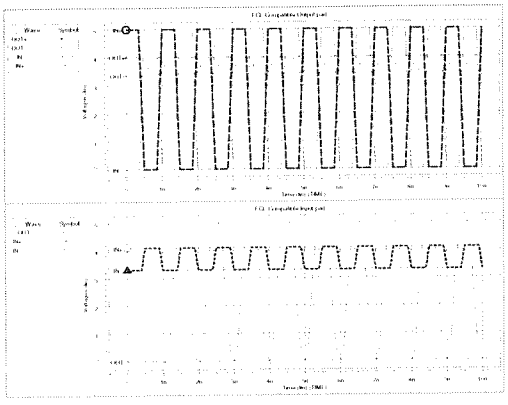

Figure 5. HSpice simulations of the I/O pads.

Further development of the proposed circuits will include:

- Use of active circuitry to dynamically increase current levels during signal transitions.
- Evaluation of temperature and voltage stability, with eventual development of self-compensation circuitry.
- Automatic matching of DC output currents to load impedances.
- Extension of these topologies to low voltage CMOS technologies.

5. Conclusions

New CMOS schemes for high performance I/O pads are proposed. Data rates up to 2 Gbit/s are supported and HSpice simulations attest the asserted performance. A test chip in ES2 0.7 μm technology have been fabricated to experimentally verify the pad working. Full speed test results are expected in a couple of months.

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