A Test Vector Ordering Technique for Switching Activity Reduction during Test Operation

P. Girard L. Guiller C. Landrault S. Pravossoudovitch

Laboratoire d'Informatique de Robotique et de Microélectronique de Montpellier,
Université Montpellier II / CNRS
161 rue Ada, 34392 Montpellier Cedex 5 FRANCE
Tél. : (+33) 467 41 86 29 Fax: (+33) 467 41 85 00 Email: <name>@lirmm.fr

Abstract

This paper considers the problem of testing VLSI integrated circuits without exceeding their power ratings during test. The proposed approach is based on the reordering of test vectors of a given test sequence to minimize the average and peak power dissipation during test operation. For this purpose, the proposed technique reduces the internal switching activity by lowering the transition density at circuit inputs. The technique considers combinational or full scan sequential circuits and do not modify the initial fault coverage. Results of experiments show reductions of the switching activity ranging from 11 % to 66 % during external test application.

1. Introduction

Power consumption has become one of the biggest challenges in high-performance VLSI design. Designers are thus continuously challenged to come up with innovative ways to reduce power while trying to meet all the other constraints imposed on the design. As a consequence, a lot of low power design techniques have been proposed at all levels of the design hierarchy. However, all these techniques focus on low power dissipation during system mode or standby mode, and do not consider the test mode.

In test mode, the switching activity of all nodes often is several times higher than the activity during normal operation [1,2]. Since heat or power dissipation in CMOS circuits is proportional to switching activity, this excessive switching activity during test can cause several problems. Firstly, this leads to an increased maximum current flow in the circuit under test (CUT) which requires a more expensive package in consequence. Moreover, with increased peak currents, electromigration becomes more likely thus affecting the reliability of the system. The relevance of this problem is still emphasized by the current trend in circuit design towards miniaturization, that prevents the use of special cooling equipment to remove excessive heat produced during test, and by the growing use of at-speed testing to identify slow chips.

The simplest way to ensure non-destructive testing of a CUT is to use test vectors or test vector ordering which cause switching activity that is comparable to that during normal circuit operation. For this purpose, several categories of techniques can be found in the literature. The first category consists of ATPG techniques [3,4], in which new ATPGs are proposed with the intent of generating test patterns able to reduce the power dissipated during test application in addition to the classical ATPG objectives. Although important reductions in switching activity can be obtained from these techniques, the main problem states in the availability of such an ATPG tool or in the time effort required to build such a tool if not available. The second category consists of Ordering techniques [5,6], in which the switching activity is reduced by modifying the order in which test vectors of a given test sequence are applied to the CUT. These techniques can be applied during external testing or deterministic BIST (Built-In Self Test), which are sole situations in which reorder test vectors of a given test sequence is possible. In the case of circuits designed with a scan path structure, the power dissipation during test operation can still be reduced by modifying the order in which the scan flip-flops are chained to form the shift register [5]. Another efficient technique presented in [2] consists in re-designing the scan cells of the scan path structure in such a way that the CUT inputs remain unchanged during shift operation.

This paper presents a new test vector ordering technique that reduces both average and peak power dissipation during test operation. For this purpose, the proposed technique reduces the total switching activity by lowering the transition density at circuit inputs. The objective is to find an optimal test vector ordering for a given test sequence such that the switching activity in the CUT is minimum. The method considers combinational circuits or full scan sequential circuits (with scan cells as those presented in [2]) and has no impact on the initial defect coverage (defects covered by the initial test sequence remain detected by the final test sequence). Compared with existing test vector ordering methods [5,6], our technique is the most time-efficient solution proposed up to now. Moreover, it considers circuit characteristics during processing thus providing better solutions in terms of amount of power saved. These features are illustrated with the experimental results gathered on the benchmarks.

0-7695-0104-4/99 $10.00 © 1999 IEEE

From a practical point of view, the test vector ordering technique proceeds as follows. First, an initial deterministic test sequence for the considered CUT is derived from the Sunrise ATPG program [7]. Next, from the signal probability on primary inputs calculated from the initial test sequence, we can compute the transition density at each input of the CUT. From these transition densities and the circuit netlist, we can then determine the value of an *induced activity function* for each input of the CUT. This function measures the impact of a transition on a specified input on the switching activity of the complete circuit. The method to calculate these functions is described in the next section. After that, test vector reordering of the initial test sequence is carried out by a heuristic method that uses the induced activity functions, thus providing an ordered final test sequence with minimum power dissipation (section 3). Experimental results reported in section 4 have shown reduction in switching activity ranging from 11% to 66% (compared with unordered test sequences).

2. Calculation of induced activity functions

In the following, we assume *spatial independence* and *temporal independence* [8].

2.1 Basic definitions

Let us consider a CUT with m primary inputs p_1, p_2, ..., p_m and n nodes x_1, x_2, ..., x_n, where n is the total number of circuit nodes that are outputs of logic gates or cells. The signal probability $P_s(x)$ at a node x is defined as the average fraction of clock cycles in which the steady state value of x is a logic high. The transition probability $P_t(x)$ at a node x is defined as the average fraction of clock cycles in which the steady state value of x is different from its initial value.

Under the *temporal independence* assumption, the transition probability can be easily obtained from the signal probability according to:

$$P_t(x) = 2.P_s(x).[1-P_s(x)] \quad (1)$$

Let $n_x(T)$ be the number of transitions at a circuit node x in a time interval of length T. Then, the *transition density* at node x, i.e. the average number of transitions per second at x, is defined as [8] :

$$D(x) = \lim_{T \to \infty} \frac{nx(T)}{T} \quad (2)$$

The transition density provides an effective measure of the switching activity in logic circuits. In a synchronous circuit with a clock period Tc, the relationship between transition density and transition probability is:

$$D(x) \geq \frac{Pt(x)}{Tc} \quad (3)$$

where equality occurs in the zero-delay case (zero-delay involves at most one single transition per clock cycle, i.e. the toggle power is not considered).

Let us now recall the concept of *Boolean difference*: the Boolean difference of the function implemented by node x, $val(x)$, with respect to input p_i is defined as:

$$\frac{\partial val(x)}{\partial p_i} = val(x)\big|_{pi=1} \oplus val(x)\big|_{pi=0} \quad (4)$$

where $\oplus$ denotes an exclusive OR operation. The transition density of a node x can be redefined in terms of the Boolean difference with respect to each input, $\partial val(x)/\partial p_i$, and the transition density of each input, $D(p_i)$, as:

$$D(x) = \sum_{i=1}^{m} P(\frac{\partial val(x)}{\partial p_i}) D(p_i) \quad (5)$$

where $P(\partial val(x)/\partial pi)$ is the probability that the Boolean difference $\partial val(x)/\partial pi$ evaluates to 1. Then, the average power dissipated in the CUT can be expressed as (eq. 6):

$$Pav = \frac{1}{2} V_{dd}^2 \sum_{\forall l} C_L(xl).D(xl) = \frac{1}{2} V_{dd}^2 \sum_{\forall l} C_L(xl) \sum_{i=1}^{m} P(\frac{\partial val(x)}{\partial p_i}).D(p_i)$$

where V_{dd} is the power supply voltage and $C_L(x_l)$ is the load capacitance at node x_l. The above equation shows that the average power dissipated in a CUT is proportional to the transition density at the inputs of the circuit. In this paper, the average and peak power dissipations during test application are reduced by lowering the transition density on the circuit inputs through test vector reordering. In the following, we make use of probability measures defined above in calculating the induced activity functions associated to each input of the CUT.

2.2 The induced activity function

In the existing test vector reordering techniques [5,6], the goal is to modify the order in which test vectors of a given test sequence are applied to the CUT so as to reduce the overall switching activity in the circuit. However, a common feature of these methods is that they focus on reducing the transition density on primary inputs only, and therefore do not consider the circuit structure and dependencies between internal nodes and primary inputs. As a result, this restriction limits the efficiency of these techniques in terms of switching activity reduction. This is explained in the following.

If a transition at an input of the CUT propagates to the internal circuit, it will subsequently cause more transitions. Depending on the circuit structure, the transitions at some inputs cause more transitions at internal nodes than those at other inputs. Therefore, reducing the transition density at some inputs must be done by measuring the impact of this reduction on the total switching activity in the circuit. In the context of our study, it means that the transition density on internal nodes must be used as a criterion during test vector reordering, rather than the transition density on primary inputs only. For this purpose, a procedure has been developed to help reorder test vectors of a given test

sequence. In this procedure, a gain function, called the *induced activity function*, is calculated for each input of the CUT. This function is based on the transition density formulation and measures the impact of reducing the transition density at a selected input on the total switching activity in the CUT. This function is now described.

The transition density of a circuit node x is the sum of the transitions at each input which propagate to node x as expressed in Equation 5. Hence, the portion of the transition density of node x due to the transition at a specific input p_i is given by:

$$Dpi(x) = P(\frac{\partial val(x)}{\partial p_i})D(pi) \quad (7)$$

where $val(x)$ is the Boolean function of node x. The sum of the transition densities of all nodes in the circuit that can be attributed to the transitions at input p_i is therefore given by:

$$Dpi = \sum_{\forall x} Dpi(x) \quad (8)$$

This function Dp_i, which takes into account dependencies between internal nodes and input p_i, could be used as gain function in our problem [9]. However, an important feature in CMOS technology is that heat dissipation in a circuit depends on the load capacitance of internal nodes, which is itself related to the fanout of the nodes. As a consequence, when two or more nodes in a CUT have the same transition density, the power induced by transitions on one node may be higher than that induced by transitions on the others, simply because the nodes may have different fanout values. For this reason, the induced activity function used as a criterion in our technique is calculated from both the transition density $Dp_i(x)$ on each node x in the circuit and the fanout $F_{an}(x)$ of the nodes. For each input p_i, this function Φp_i is given by:

$$\Phi pi = \sum_{\forall x} Dpi(x).Fan(x) \quad (9)$$

This gain function Φp_i is computed for all inputs of the CUT in the following manner:

$$\Phi pi = \sum_{\forall x} P(\frac{\partial val(x)}{\partial pi}).D(pi).Fan(x) \quad (10)$$

$$\Phi pi = \sum_{\forall x} P(\frac{\partial val(x)}{\partial pi}).fclock.Pt(pi).Fan(x) \quad (11)$$

The final expression of Φp_i as used in the procedure discussed above is as follows (eq. 12):

$$\Phi pi \cong \sum_{\forall x} P(\frac{\partial val(x)}{\partial pi}).Pt(pi).Fan(x) \text{ with } P_t(p_i) = 2.P_s(p_i).[1-P_s(p_i)]$$

In this expression, the fanout on node x, $F_{an}(x)$, is directly obtained from the circuit structure. The transition probability on input p_i, $P_t(p_i)$, is calculated from the signal probability on p_i (see Equation 1). The signal probability on input p_i, $P_s(p_i)$, is calculated from the initial deterministic test sequence by counting the number of 0s and 1s in the i-th bit position of the vector sequence. More formally, the signal probability on input p_i is given by:

$$P_S(pi) = \frac{\#\text{ vectors in TS with pi = 1}}{\text{total \# vectors in TS}} \quad (13)$$

The probability that the Boolean difference of $val(x)$ with respect to p_i evaluates to 1, $P(\partial val(x)/\partial pi)$, is derived from the signal probability of each node using a procedure similar to what is used to calculate detection probability in [10]. Details about this procedure can be found in [9].

3. Solving the test vector ordering problem

According to the above discussion, the problem considered in this paper amounts to compute an optimal vector ordering of a test sequence TS such that both the average power and the peak power dissipation in the circuit are minimized. To solve this problem, consider a complete undirected graph G=(Ψ,E) in which each vertex $V_k \in \Psi$ represents a test vector of TS and each undirected edge $(V_{k-1},V_k) \in E$ represents a pair of test vectors. The weight on each edge (V_{k-1},V_k) represents the cost in terms of transition density of the application of the pair (V_{k-1},V_k) to the CUT. The weight on edge (V_{k-1},V_k) can be formally defined as:

$$Weight(Vk-1,Vk) = \sum_{i=1}^{m} \Phi pi.[val(pi,Vk-1) \oplus val(pi,Vk)] \quad (14)$$

where $val(p_i,V_k)$ represents the value on input p_i when vector V_k is applied to the CUT, and the Boolean difference $val(p_i,V_{k-1}) \oplus val(p_i,V_k)$ is equal to 1 if there is a transition on input p_i between V_k and V_{k-1}, and 0 otherwise. In other words, the weight on each edge of G is obtained by summing the values of the induced activity function of inputs changing from 1 to 0 or 0 to 1 after application of test pair $TP_k=(V_{k-1},V_k)$.

After that, computing an optimal vector ordering of the test sequence that minimizes the power dissipation during test application amounts to finding an Hamiltonian path of minimum cost in the complete graph G. In this case, the cost of a path is obtained by summing the weights of edges belonging to the path. This problem is equivalent to the well known traveling salesman problem (NP-hard) for which different polynomial-time approximation algorithms can be used [11]. Among these solutions, greedy algorithms represent a good tradeoff between computation time and efficiency of the computed solution. We therefore implemented an heuristic solution based on an improved greedy algorithm.

Compared with the method proposed in [5], our technique does not need to simulate the considered circuit for all possible pair of vectors in the test sequence. This is performed in [5] so as to construct the transition graph from which an hamiltonian path is searched. Our technique hence allows to deal with test sequences of practical and

great length, thus allowing to consider complex VLSI circuits. Compared with the method proposed in [6], the proposed technique takes into account dependencies between internal nodes and primary inputs and therefore provides more efficient solutions in terms of amount of power saved

4. Experimental results

Benchmarking process was performed on combinational circuits from the ISCAS'85, ISCAS'89 (combinational part of sequential circuits), and MCNC'93. The improved greedy algorithm has been implemented in the C++ language, and all the experiments have been run on a SunSPARC-5 workstation. The zero delay model was used for the gates in each circuit.

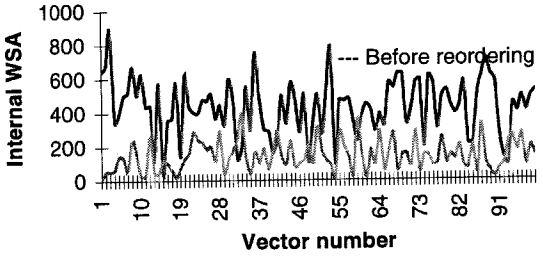

Figure 1: Comparison between WSA before and after reordering - circuit s1488

A first sample of the results obtained is depicted in Figure 1 for ISCAS'89 circuit s1488. The internal WSA (Weighted Switching Activity) is reported before and after reordering of the initial deterministic test sequence. The WSA is the product $S_w(x).F_{an}(x)$ of the switching activity and the fanout of node x, and is used as a metric for the power consumption at that node, since it is the only variable part in the power consumed during test pattern application. Each value on the X-axis represents a vector of the test sequence (and hence one clock cycle) and each value on the Y-axis represents the internal WSA (the WSA of the CUT's internal nodes) generated in one clock period. These results highlight the reduction in average switching activity for this circuit, as well as the reduction in peak power dissipation as announced in section 1.

Complete results are summarized in Table 1 for each benchmark circuit. The two first columns in Table 1 list the name of the circuits and the number of vectors in the deterministic test sequence respectively. For each of these circuits, the fault coverage achieved with the deterministic test sequence is the maximum stuck-at fault coverage of detectable faults (100 %). The test sequence were generated by using the deterministic ATPG tool of Sunrise Test System [7]. The next columns report the internal WSA before (*initial WSA*) and after (*final WSA*) test vector reordering. For each circuit, these values represent the summing of the internal WSA over all vectors of the test sequence. The ratio between internal WSA before and after reordering is reported in the last column (Gain in %).

Circuit	# vect	Init. WSA	Final WSA	Gain
rd73	128	21276	9517	55 %
clip	167	45658	19241	57 %
sao2	125	15449	7379	52 %
c5315	88	154257	136314	11 %
c7552	118	266362	219246	17 %
s420	64	5069	3605	28 %
s510	70	10332	4678	54 %
s820	142	39278	16558	57 %
s832	144	40368	16948	58 %
s1238	176	54464	29811	45 %
s1488	151	79918	27004	66 %

Table 1: Complete results of test vector reordering

From the results given in Table 1, we can see that about 37.6 % reduction in switching activity has been obtained on the average, with a maximum of 66 % for circuit s1488. These results demonstrate the interest and the effectiveness of the proposed technique in terms of amount of power saved during test operation. The proposed technique reduces not only the average power dissipation but also the peak power dissipation, thus minimizing the risk to damage the CUT during testing. The complete algorithm proceeds very swiftly and can therefore be used as a postprocessing tool in preparing the test programs for a complex VLSI device.

References

[1] Y. Zorian, « A Distributed BIST Control Scheme for Complex VLSI Devices », IEEE VLSI Test Symp., pp. 4-9, April 1993.

[2] A. Hertwig and H.J. Wunderlich, « Low Power Serial Built-IN Self-Test », IEEE European Test Workshop, pp. 49-53, May 1998.

[3] F. Corno, P. Prinetto, M. Rebaudengo and M. Sonza Reorda, « A Test Pattern Generation Methodology for Low Power Consumption », IEEE VLSI Test Symp., pp 453-459, May 1998.

[4] S. Wang and S.K. Gupta, « ATPG for Heat Dissipation Minimization During Test Application », IEEE Int. Test Conf., pp. 250-258, 1994.

[5] S. Chakravarty and V.P. Dabholkar, « Minimizing Power Dissipation in Scan Circuits During Test Application », IEEE Int. Workshop on Low Power Design, pp. 51-56, April 1994.

[6] P. Girard, C. Landrault, S. Pravossoudovitch and D. Severac, « Reducing Power Consumption during Test Application by Test Vector Ordering », IEEE Int. Symp. on Circuits and Systems, CD-Rom proceedings, June 1998.

[7] SUNRISE Test System, Version 2.3.b, May 1997.

[8] F.N. Najm, « Transition Density, a Stochastic Measure of Activity in Digital Circuits », ACM Design Auto. Conf., pp. 644-649, June 1991.

[9] S. Wang and S. Gupta, « DS-LFSR: A New BIST TPG for Low Heat Dissipation », IEEE Int. Test Conf., pp. 848-857, November 1997.

[10] P.H. Bardell, W.H. McAnney and J. Savir, « Built-In Test for VLSI: Pseudo-Random Techniques », John Wiley & Sons, 1987.

[11] D.S. Johnson and L.A. McGeoch, « the Traveling Salesman Problem : A Case Study in Local Optimization », in Local Search in Combinatorial Optimization, E.H.L. Aarts and J.K. Lenstra, eds. John Wiley and Sons, 1996.