

## Panel: Taming noise in deep submicron digital integrated circuits

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As technology scales into the deep submicron regime, noise immunity is becoming a metric of comparable importance to area, timing, and power for the analysis and design of digital VLSI chips. Are functional failures due to noise really a problem in a static CMOS design? Are design rules in the circuits and interconnect sufficient to protect against noise failures? Do design rules targetted to ensure noise immunity result in excessive penalty to performance and area due to their inherent conservatism? Is inductance in the interconnect really a problem? How much do we really need to account for capacitive coupling, inductance, and inductive coupling in delay analysis?

**Chris Houghton, Digital Equipment Corporation, Hudson, MA** For years the digital IC design community has analyzed on-chip interconnect for capacitive and resistive effects. This has been done for both timing (capacitive loading on local interconnect and RC analysis of longer signals) and to assure integrity (capacitive coupling analysis). This is direct recognition that functional failures due to noise really are a problem.

Approaching the problem of on-chip noise with an armada of design rules does not assure success. Design rules are certainly necessary as the basis for any good design but they are not sufficient to protect against failures due to noise. An example of a "design rule" that no longer assures success is that of using only static CMOS circuit topologies. Although static circuits can have significantly more noise immunity than dynamic structures, in today's technologies (where coupled loading is a large portion of total loading) static structures can also fail. Even if static circuits mitigated all worry of noise, exclusive use of static design is often not an option in high performance circuits.

No rule set will, on its own, assure the integrity of a design. Even if it could, there certainly would be a penalty in circuit size, performance or power. Detailed circuit analysis is required to isolate timing and "signal integrity" problems. Given the large number of circuits on today's chips, the bulk of this analysis must be done with the help of EDA tools.

With the operating frequencies of ICs reaching the point where multi-Gigahertz on-chip interconnect bandwidths are required to accurately propagate signals, the question of what, beyond the standard RC analysis of yesterday, is needed today (and certainly tomorrow!) is raised. A popular question concerning on-chip signaling these days is: "is inductance in the interconnect really a problem?". The answer is "yes", but "maybe" is also valid. Recent improvements in the conductivity of on-chip metalization do not necessarily lessen the problems with inductance. In fact, in some situations higher conductivity interconnect can amplify the inductive effects. If the IC's "physical architecture" does not properly accommodate signal current return paths and does not control mutual inductance effects, then the answer is "yes, inductance is a problem" for even the 500 MHz designs of yester-

day. The answer is a softer "maybe" for some "local" on-chip interconnect if the designer assures at least minimal accommodation of signal returns and minimization of coupled loading (w.r.t. self loading). This is true even in designs over 1 GHz designs.

Technology has come to our rescue in the past and hopefully will continue to in the future. Finer pitch interconnect and extra metalization layers have allowed for direct inclusion of reference structures (signal return paths). Recent and/or planned CMOS technology features will further ease high frequency design constraints, (e.g. higher conductivity on-chip metalization, low- $\kappa$  dielectric layers and SOI). Flip-chip packaging has reduced the maximum length of global on-chip interconnects, reduced on-chip power supply noise and on-chip global clock skew. However, before we rely solely on technology as the panacea, consider the improvements that present design and analysis techniques yield within any given set of technology constraints.

**Barbara Chappell, Intel Corporation, Hillsboro, OR** With the shrinking voltages and increasing currents in deep-submicron IC's, performance for many important applications is too severely compromised by the usual worst-casing methods for assuring noise margins. However, modeling noise effects with sufficient accuracy to allow relieving of worst-case costs is difficult to do in any general way. What is the correct approximation model and analysis method is dependent on many design-specific elements - such as the circuit topologies to be supported, the performance targets, and the design optimization methods. Consequently, CAD developers need to work closely with designers in making their design tools noise-aware.

**Xiaonan Zhang, Metaflow Technologies, Inc., La Jolla, CA** As CMOS technology advances, intrinsic gate delay decreases and interconnect wire delay increases with respect to overall circuit delay. The coupling capacitance between minimum pitch wires on a 0.25 $\mu\text{m}$  CMOS IC can account for over 80% of the total capacitance of a wire. This makes interconnect crosstalk noise one of the biggest challenges in VLSI design today. I will discuss this noise problem from a circuit designer's point of view.

Crosstalk due to capacitive coupling is a complex phenomenon. One type of coupling-capacitance-

induced crosstalk noise can be pervasive in today's interconnect intensive VLSI chips. It can occur in the following manner. When the voltage of an aggressor signal changes as the voltage of a victim signal is in transition through the high gain region of a receiver circuit (This is near  $V_{DD}/2$  in a typical static CMOS design), if the switching directions are opposite of each other, a ripple or a small glitch is formed in the victim signal. This "high-gain crosstalk" can affect a circuit in many different ways:

- In a static CMOS design, this glitch increases the wire delay considerably (the signal goes across the receiving threshold back and forth). It also increases the receiving circuit delay since it alters the effective input rise/fall time. This causes speed-related logic errors.
- Sometimes, the receiving circuit amplifies the glitch to a larger glitch. This causes failures in edge-sensitive logic. The glitch can propagate through many gates.
- If the signal feeds into a dynamic logic gate, it can discharge the storage charge during the evaluation phase and cause a logic error.

Capacitive-coupling-induced interconnect crosstalk noise is a major problem in deep sub-micron VLSI design. The worst noise problem is high gain crosstalk. Circuit design techniques may provide viable solutions to the problem. However, this requires mostly custom design solutions. It is important to realize, crosstalk due to coupling capacitance between different wires on a chip is not simply a signal integrity problem, it can cause several other types of failures. We have observed the effects of crosstalk not only in dynamic circuits and analog circuits but also in static digital CMOS circuits. Minimizing crosstalk noise has become a major challenge to today's CAD tool developers and circuit designers. Copper wires will alleviate the problem to a certain extent. However, they do not eliminate the problem. High gain crosstalk will remain a challenge to engineers and scientists working on deep sub-micron and future generation VLSI designs.

**John MacDonald, Sun Microsystems, Palo Alto, CA** With metal trace dimensions a small fraction of a micron and rise and fall times a small fraction of a nanosecond, both capacitive and, to some degree, inductive coupling between signals become a significant problem for digital CMOS designs.

While most designers are aware of the damage that noise can do to the functionality of dynamic or pre-charged circuits, coupling noise can also cause functional failures in static CMOS. The effect that coupling has on propagation delay is fairly well understood but remains poorly modeled. As capacitive coupling is becoming the dominate component of interconnect loading, the standard practice of modeling it as a grounded capacitor with a "Miller" multiplier is becoming a leading source of inaccuracy in modeling delay. While we are not yet seeing significant problems on chip with inductive effects such as ringing or reflection, inductive coupling between signals is sometimes significant and should also be considered.

With diligence, design rules can be established and verification tools utilized to keep designs out of trouble. Nevertheless, the cost in area and performance is high, particularly considering the conservatism that design rules and tools rely upon.

**John McBride, Hewlett-Packard, Fort Collins, CO** Controlling "noise" has long been a concern of digital circuit designers. Whether that noise be radio-frequency-interference (RFI) noise, voltage supply noise, or signal integrity, noise has always been a concern. It is nothing new. PC board designers have been dealing with noise issues for a long time. Now signal speeds have increased and spacing has decreased to the point where digital ICs are highly susceptible to noise, too. The first coupling to show up is capacitive coupling, and the extraction and analysis of capacitive couple is fairly established at this point. Because designers have a knowledge of capacitive coupling, they know not to route long lines on inputs to dynamic gates, diffusion inputs to latches, and other sensitive circuits. Even static logic is becoming more susceptible to all types of noise as the supply voltage drops to 2.5V and beyond. Designers can take methodological steps to prevent capacitive coupling, and then use analysis to see if they were right, and if there are any hidden problems. There can always be improvements in the way designers analyze coupling, but compared to other problems in developing digital ICs, capacitive coupling is well understood and can be thoroughly analyzed.

Inductive coupling in digital ICs is another story. The extraction of inductance is painfully slow. Extracting the inductance of all the signals on a large IC is completely infeasible at this time. Yet, inductance has been shown to be at least a contributing factor in the electrical problems of some current high-speed ICs. As signal edge rates increase, inductive coupling will get worse. Even though copper interconnect make inductance easier to eliminate, copper will not be available to most designers for quite a while. Even then, inductance will still be a concern. Like capacitive coupling, many of the instances of inductive coupling can be stopped by methodology used in the design. Unlike capacitive coupling, the methodology is virtually the only way, today, to eliminate inductive coupling problems. With every process, the design team needs to analyze the process for inductive coupling, and the team needs to carefully select the right guidelines for wire spacing, wire width, metal fill, wire length, ground returns, etc. These guidelines should be applied by all circuit designers, and checked for adherence to the guidelines. All "long" nets that drive sensitive circuitry should be extracted and analyzed. ("long" is defined by the design team). Attacking the problem primarily through the methodology has inherent downsides, namely that performance and signal density will suffer unnecessarily on some signals, unnecessary work will be performed on some signals, and there will always be some signals that are missed. However, until the extraction and analysis of inductive coupling catch up to where capacitive coupling are today, methodology will continue to be the primary defense against inductive coupling.

**Bob Masleid, IBM, Austin, TX** No advance position statement.