Extension of the Boundary-Scan Architecture and New Idea of BIST for More Effective Testing and Self-Testing of Interconnections.

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Abstract

The approach presented in this paper enables more effective testing of on-board and board-to-board interconnections and significantly simplifies the interconnection self-testing. Some extensions must be added to the Boundary Scan Architecture which however do not violate the JTAG/IEEE1149.1 standard requirements. Benefits are the reduced complexity and cost of an on-board testing unit as well as better test performance.

Summary

The proposed idea of BIST enables easy and reliable testing of interconnections. A BIST mechanism, normally reserved for testing cores of ICs, in this case is used for testing exterior of ICs, a set of interconnections. The proposed BIST, let us call it INETBIST, is intended to be a part of the Boundary-Scan Architecture, [1]. It is assumed that the Split Boundary-Scan Registers, [2], are implemented. To achieve the optimal test generator the Output B-S Registers of particular ICs are arranged into a single chain using standard TDI and TDO terminals, see Fig.1.

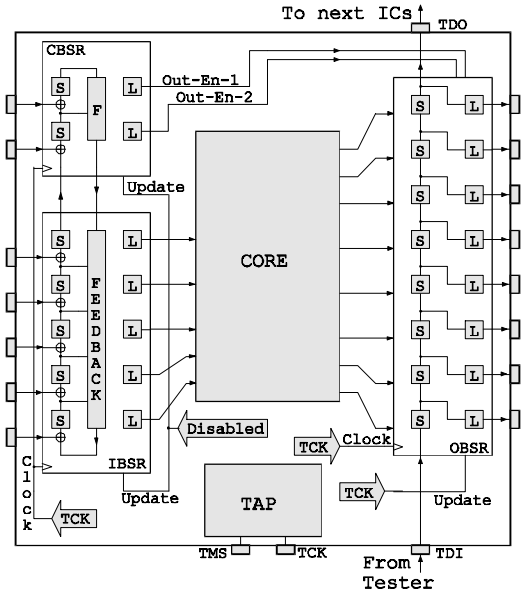

Figure 1: IC operating in the INETBIST mode.

Input and Control B-S Registers are designed to perform compaction of a test response. The following pseudocode describes a process of detection of interconnection faults:

PSEUDOCODE: Self-Test of Interconnections;
INITIALIZE all Boundary-Scan Registers;
SELECT the INETBIST instruction;
FOR EVERY valid control vector
{ *UPDATE* Control B-S Registers;
PERFORM n_i TCK pulses of INETBIST; }
READ the result of test
& *COMPARE* with the stored correct one;
END of PSEUDOCODE.

In most cases a number of the valid control vectors is small, so the test task is very simple, and a very simple test controller (master) is required. Since the effect of serially exchanged long test vectors is almost eliminated the INETBIST is significantly less time consuming compared to the traditional way of testing.

The reliability of interconnection testing will reach extremely high level if modified output stages are implemented, [3], [4]. They guarantee demanded fault model for both single and multiple faults. Additionally, they will enable true full diagnosis in the traditional way of testing. Detection of dynamic interconnection faults (delays) is possible provided that the test clock frequency can be increased up to the normal board or system operating speed. The on-line short-circuit detecting output stages presented in [4], if used, can aid the concurrent testing.

References

1. IEEE Standard 1149.1-1990, "Standard Test Access Port and Boundary-Scan Architecture", IEEE Standards Board, New York 1990.

2. Nazar S. Haider & Nick Kanopoulos - "The Split Boundary Scan Register Technique for Testing Board Interconnects", IEEE VLSI Test Symposium 1992, Paper 2.3, pp. 43-48.

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