

Estimation of the Number of Routing Layers and Total Wirelength in a PCB Through Wiring Distribution Analysis

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Abstract

This paper describes a model to estimate the number of routing layers and total wirelength for a printed circuit board given the netlist, partslist, placement and board form factor. The estimation model is based on analysis of the wiring distribution on the board. The wiring distribution consists of the net distribution and net segmentation. An algorithm is presented which determines the contribution of net distribution. A statistical model has been developed to estimate net segmentation as “wrong way” routes due to obstacles and congestion on a board. Routability estimations are substituted for the routing task while searching the design space, significantly reducing the design time since routing is the most time consuming design task. These estimation techniques have been successfully applied to the board estimations of several designs, including a multiprocessor printed circuit board and the results are presented here.

1.0 Introduction

With the increasing demand for rapid prototypes of electronic systems, the design of printed circuit boards (PCB) has emerged as a bottleneck in the design cycle. Reducing the design time and cost of a PCB are the two main rapid prototyping design objectives. The most significant factor affecting the cost of a design is the number of routing layers.

Designers usually perform several design iterations varying the placement and number of routing layers to determine a minimum cost board that is 100% routable. Even when 100% routing is achieved, the performance may be poor due to a component placement that does not sufficiently reduce the total wirelength. Minimizing the total wirelength of a design is an important performance criteria [5] [6]. Design time constraints restrict the number of iterations that can be tested, reducing the chances of finding an “optimal” board design. Thus 100% routing may be achieved at the cost of performance and using more layers than required.

In order to achieve a board design with the minimum required number of routing layers and minimum total

wirelength, while reducing the design time, estimates of the required number of routing layers and total wirelength are needed, as shown in Figure 1.

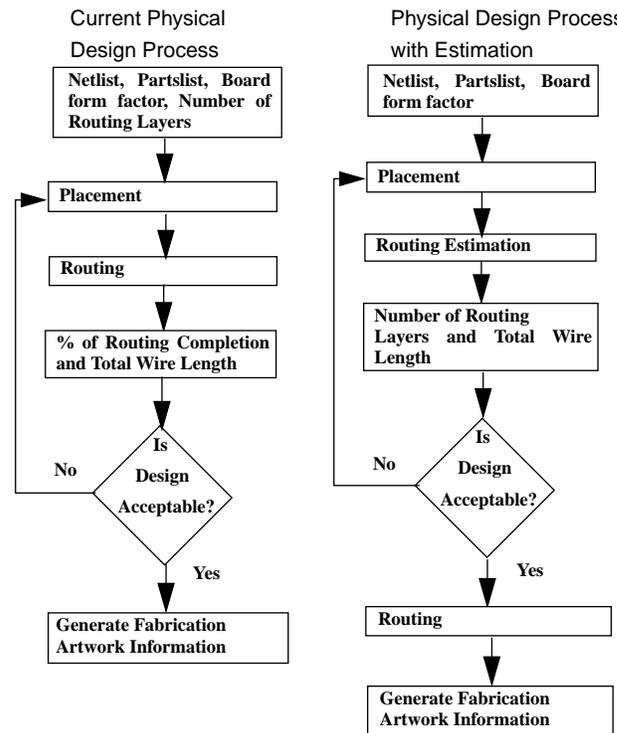


Figure 1. Comparison of Physical Design Processes

2.0 Related Research on Board Estimation and Routability

Early research was performed by Sutherland and Oestricher [1] in estimating the minimum form factor of a custom sized PCB. In rapid prototyping, where the emphasis is on time-to-first-artifact it is advantageous to use a standard board type with its associated connector pin-out and form factor. A standard board type fixes the form factor but allows the designer to add layers to achieve 100% autorouting. Therefore, the problem we address in this paper is estimating the minimum number of routing layers.

The graphical display of unconnected nets on the board or

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“rats nest”, shown in Figure 2, is a widely used routability indicator supplied by commercial computer-aided design tools [4] [7]. Areas of dense wires and crossings indicate areas of high wiring congestion that may be unroutable. Designers rely on experience to correctly interpret the “rats nest” because it is qualitative and not expressed in a computer processable form. Often the “rats nest” is decomposed into horizontal and vertical projections of the wiring distribution, as shown in Figure 2. The horizontal and vertical wiring distributions show the minimum number of wiring tracks needed to route the design. During the decomposition process, one loses information about the specific horizontal and vertical location a net will cross the board.

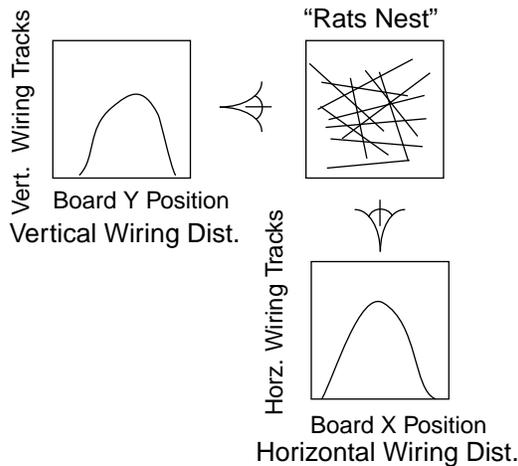


Figure 2. “Rats Nest” and Projections into Horizontal and Vertical Wiring Distributions

Foster [2] used the wiring distributions for routability prediction by observing that to achieve 100% routing completion, a board must have at least the same number of available wiring tracks as the maximum value of the wiring distribution diagram. This observation is based on a simplified view of the required number of routing tracks by assuming a uniform distribution of wires throughout a board and ignoring the interference and congestion caused by closely spaced wiring tracks, component pins and vias. Foster did not consider congestion caused by vias because PCB technology at that time placed vias in predefined columns and rows on a board resulting in a less efficient route. Current board level routing tools dynamically place vias on the board during the routing process.

Foster’s wiring distributions work well for simple designs of two pin nets and dual in-line packages placed in regular arrays. But these wiring distributions are not generally applicable to current board designs with multi-pin nets and an assortment of complex packages, such as pin grid arrays with over 300 pins.

A second approach by Schmidt [3] uses an analytical wiring distribution model to estimate the maximum value of the

horizontal and vertical wiring distributions. This analytical wiring distribution model does not use the component placement as an input, but relies on an idealized model of component placement that locates those components most strongly connected to the connector in closest proximity to the connector. The Schmidt wiring distribution model assumes a decreasing distribution of the number of nets away from the connector. We have examined several test case boards and have found this model to be inadequate. Furthermore, both Foster’s algorithm and Schmidt’s model assume a simplified view of the required number of routing tracks by ignoring the interference and congestion caused by closely spaced wiring tracks, component pins and vias, as described in Section 3.0.

3.0 Estimation Approach for Wiring Distribution

As the “rats nest” is decomposed into horizontal and vertical wiring projections, a similar decomposition technique can be performed on a completely routed board to determine the number of horizontal and vertical wiring tracks actually used. The resulting horizontal and vertical wiring distribution diagrams show the number of wire crossings for each horizontal and vertical position on the board, as seen in Figure 3. Wiring distribution diagrams are made up of two components, the net distribution which is the minimum number of horizontal and vertical wiring tracks to fully interconnect a net, and the net segmentation which are “wrong way” routing paths that use an additional number of wiring tracks as depicted in Figure 4. In Figure 4, the net distribution indicates the minimum required number of tracks to route the net, while the actual route contains additional tracks needed by net segmentation to avoid an obstacle. The net distribution is determined by the position of the pins in the nets during the placement process. The net segmentation is caused by the presence of obstacles and congestion; such as pins, vias, and closely spaced wiring tracks. Our analysis finds that net segmentation comprises 10% - 35% of the wiring distribution values, as shown in Figure 3. This contribution to the required number of tracks is completely ignored in Foster’s as well as Schmidt’s estimation techniques.

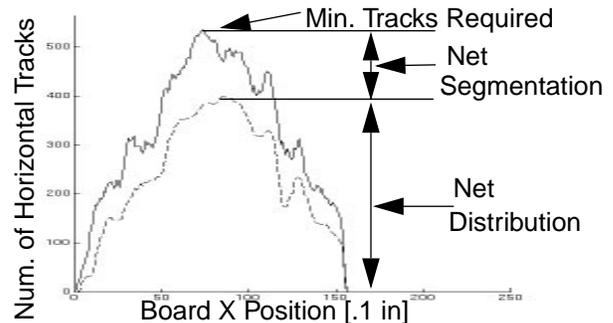


Figure 3. Wiring Distribution Consists of Net Distribution and Net Segmentation

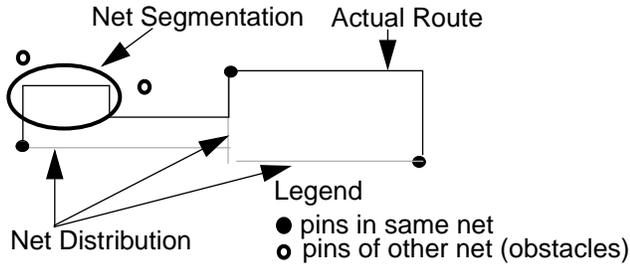


Figure 4. Net Distribution and Net Segmentation

Net segmentation is modeled as a probabilistic process due to the dynamic placement of vias and congestion that result from the routing process. The routing of nets is performed as a spanning tree, so the routing of net i needs to consider the obstacles and congestion caused by the routing paths of nets $i-1$, $i-2$, to i . The alternate routing paths may use a different number of horizontal and vertical wiring tracks, as seen in Figure 5. It is seen that a trade-off exists between the number of horizontal and vertical routing tracks used for both of these alternative routing paths. For each of the possible routing paths the net distribution remains the same since at least one wiring track must be used in the horizontal and vertical layers to route the net. The net segmentation model takes into account the trade-off between the additional number of routing tracks used in the horizontal and vertical layers to avoid obstacles.

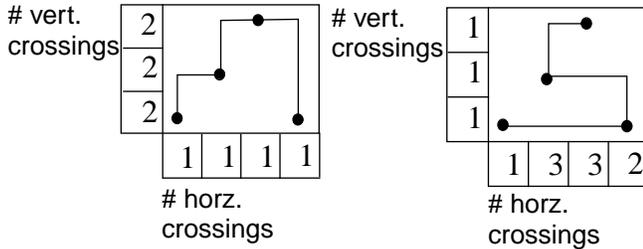


Figure 5. Two Different Net Segmentation Schemes

4.0 Net Distribution

Net distribution is determined by the following algorithm.

Net Distribution Algorithm: Given a netlist, partslist, placement of the components and board form factor.

- Step 1* Divide the board into horizontal and vertical strips and initialize counter for each strip.
- Step 2* Select a net in the design, if no more nets to be selected, go to Step 5.
- Step 3* Identify the pin locations of the net and calculate bounding box encompassing all pins in the net.
- Step 4* Increment counter for each horizontal and vertical strip spanned by bounding box, go

to Step 2.

- Step 5* Output horizontal strip counter values as horizontal net distribution and vertical strip counter values as vertical net distribution.

5.0 Net Segmentation

A net segmentation model is developed in Section 5.1 to estimate the additional number of wiring tracks needed for routing around obstacles such as pins and vias, and to avoid areas of high wiring congestion.

5.1 Net Segmentation Model

The net segmentation model is defined as a linear combination of the contributions from each different type of obstacle as shown below:

$$f(n, p, v, w, c) = a_0 + a_1n + a_2p + a_3w + a_4v + a_5c \quad (1)$$

Where:

- n = Value calculated by net distribution algorithm for strip, indicates amount of wire crossings in a board strip, see Section 4.0.
- p = Number of pins in a horizontal or vertical strip, indicates amount of routing obstacles in a board strip.

$$w = \forall \left(\sum \left(\forall \left(\frac{1}{\text{bounding box width}} \cdot \frac{1}{\text{bounding box length}} \right) \right) \right) \text{ strip net bounding box}$$

Characterizes the wiring congestion of each board strip.

- v = Estimate of the number of vias in a strip. This value is estimated because it is a result of the routing process.

$$c = \forall \left(\sum \left(\frac{1}{\text{distance between pins and vias}} \right) \right) \text{ strip}$$

Measures the density of pins and vias for each board strip.

The model variables w , v , and c can be determined as described below.

5.1.1 Net Density Algorithm to Determine w

Given a netlist, partslist, placement of the components and board form factor:

- Step 1* Divide the board into horizontal and vertical strips, create boxes for each of the intersections of the horizontal and vertical strips, and initialize counters to each box and strip.

- Step 2* Select a net in the design, if no more nets to be selected, go to Step 5.
- Step 3* Identify the pin locations of the net and calculate bounding box encompassing all pins in the net.
- Step 4* Calculate n and m to be the length and width of the bounding box, respectively. Multiply $1/n$ and $1/m$, add value to each box in bounding box. Go to Step 2.
- Step 5* For each horizontal and vertical strip, sum up the values of boxes in the strip to obtain value of w .

5.1.2 Via Estimation Algorithm to Determine v

Given a netlist, partslist, placement of the components and board form factor estimate the location of vias on the board as follows:

- Step 1* Divide board into horizontal and vertical strips, and initialize counter for each strip.
- Step 2* Select a net in the design, if no more nets to be selected, go to Step 7.
- Step 3* Identify pin locations of the net. Order pins from left to right, and determine the two rectilinear paths to connect each pair of adjacent pins.
- Step 4* Identify potential via locations as bends in paths between adjacent pins.
- Step 5* Compare value of net density for both potential via locations between adjacent pins, select via location corresponding to lower value of net density.
- Step 6* Increment corresponding counter, go to Step 2.
- Step 7* For each horizontal and vertical strip, sum up counter values for each strip to obtain value of v .

5.1.3 Pin and Via Density Algorithm to Determine c

Given a netlist, partslist, placement of the components and board form factor determine the density of pins and vias on the board as follows:

- Step 1* Divide the board into horizontal and vertical strips, initialize counter for each strip.
- Step 2* Perform Via Estimation Alg. Steps 2 - 6 to locate via locations, locate pins from placement.
- Step 3* For each strip in board, count distance between pins and vias in a strip, calculate and sum $1/(\text{distance between pins and vias})$ to obtain value of c .

5.2 Net Segmentation Model Development

The models for the horizontal and vertical tracks are developed separately to reflect the unequal contribution of obstacles to the additional wiring tracks.

Multiple regression least squares analysis was performed on six test cases to determine the coefficients of the net segmentation model (Equation 1 in Section 5.1).

Given: \bar{y} = actual wiring distribution
 \bar{X} = test case values of variables $n, p, w, v,$ and c
 the coefficient vector \bar{a} is determined as:

$$\bar{a} = (\bar{X}^T \bar{X})^{-1} \bar{X}^T \bar{y}$$

The resulting values for the horizontal and vertical model coefficients are shown in Table 1. The values for the maximum number of horizontal and vertical routing tracks were calculated using the proposed model and compared to the actual values for each test case. The errors were analyzed statistically for Foster's algorithm, Schmidt's model and the model presented here. The results are shown in Table 2.

5.3 Net Segmentation Model Validation

The coefficient of multiple determination is one measure used to validate a multiple linear regression model. R^2 is a measure of the amount of reduction in the variations of the predicted value obtained by using the regression variables $n, p, w, v,$ and c .

$$R^2 = 1 - \left(\frac{SSE}{S_{yy}} \right)$$

$$SSE = \sum_{i=1}^n (y_i - \hat{y}_i)^2$$

$$S_{yy} = \bar{y}^2 - (1/n) \left(\sum_{i=1}^n (y_i) \right)^2$$

As in simple linear regression, we must have $0 \leq R^2 \leq 1$. However, a large value of R^2 does not necessarily imply the regression model is a good one. The fact that R^2 is close to 1 and the predictions have a small error validates the proposed model.

6.0 Routing Layer Estimation

Given an estimate of the number of horizontal and vertical wiring tracks for a design and the number of wiring tracks available on a board, we can estimate the required number of routing layers.

$$\# \text{ Routing Layers} = \left(\frac{\text{Estimated \# Wiring Tracks}}{\text{Available \# Wiring Tracks/ layer}} \right)$$

The estimated maximum number of the horizontal and vertical wiring distribution values are divided by the number of wiring tracks available per layer to determine the required

number of routing layers. The average % error of the estimated required number of horizontal and vertical routing layers are given in Table 2. It is seen from Table 2 that routing layer estimates from the proposed model are five and two times more accurate than Foster and Schmidt's estimates, respectively.

7.0 Total Wirelength Estimation

From the estimates of horizontal and vertical wiring distributions, the total wirelength of a design is the area enclosed in the wiring distribution curves.

$$\begin{aligned} \text{Total Horizontal Wirelength} &= \int_{\text{left board edge}}^{\text{right board edge}} \text{Horizontal Wiring Distribution} \\ \text{Total Vertical Wirelength} &= \int_{\text{top board edge}}^{\text{bottom board edge}} \text{Vertical Wiring Distribution} \\ \text{Total Wirelength} &= \text{Total Horizontal Wirelength} + \text{Total Vertical Wirelength} \end{aligned}$$

Shown in lines 5 and 6 of Table 2 are the average % error for the predicted total wirelength for the horizontal and vertical layers, respectively. It is seen from Table 2 that the total wirelength estimates with the proposed model are three and six times more accurate than Foster's and Schmidt's estimates, respectively.

8.0 Example Multiprocessor Benchmark

Testing a model on the same data that developed the model does not ensure the accuracy of the model for other designs. A separate multiprocessor board design (*db1*) was used as a benchmark to compare the accuracy of the proposed model against the accuracy of Foster's algorithm and Schmidt's model. The proposed model results in a 2% error for both the maximum number of horizontal and vertical tracks, 0% error for the number of horizontal and vertical routing layers, and 1% and 4% error for the total horizontal and vertical wirelength, respectively. By contrast Foster's and Schmidt's estimates have errors consistently within 25% and 33%, respectively. Figure 6 shows the accurate tracking of the actual horizontal wiring distribution by the proposed model.

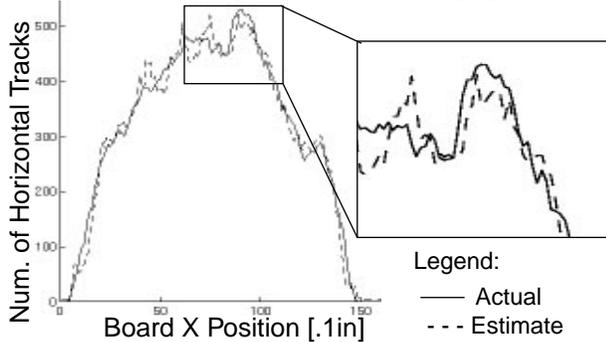


Figure 6. Actual Wiring Distribution and Estimated Wiring Distribution

9.0 Net Segmentation Model as an Estimator

9.1 Stability of Net Segmentation Model

A statistical model has two figures of merit:

$$\text{Mean error} = 1/n \cdot \sum_{i=1}^n (y_i - \hat{y}_i)$$

$$\text{Standard deviation} = \sqrt{1/n \sum_{i=1}^n (y_i - \hat{y}_i)^2}$$

The statistical model is said to be *stable* if the mean error is less than 5% and the standard deviation is less than 10% [8]. The mean error of the multiple linear regression fit applied back to the test cases is 0% for the horizontal direction and 1% for the vertical direction. The standard deviation is 9% for the horizontal direction and 10% for the vertical direction. Therefore, the net segmentation model is *stable* and can be used as a predictor for the net segmentation of other designs.

9.2 Confidence Interval of the Net Segmentation Model

The 95% confidence intervals of the coefficients of the proposed model have been calculated as shown below:

$$\hat{C}_i - t_{\alpha/2, n-p} \cdot \sqrt{\hat{\sigma}^2 C_{jj}} \leq C_i \leq \hat{C}_i + t_{\alpha/2, n-p} \cdot \sqrt{\hat{\sigma}^2 C_{jj}}$$

Where:

\hat{C}_i = Multiple linear regression fit model coefficient

C_i = Model coefficient

$\hat{\sigma}^2$ = Variance

C_{jj} = jjth element of $(\bar{X}'\bar{X})^{-1}$

$t_{\alpha/2, n-p}$ = t distribution value

Table 1 lists the confidence intervals of the multiple linear regression fit coefficients. The upper and lower limits of the 95% confidence interval have been used to calculate the errors for the *db1* benchmark design. The results are 8% and 4% error on estimates of the maximum wiring distribution values, 0% error in estimating the number of both the horizontal and vertical routing layers, and 18% and 7% error in estimating the total wirelength. The application of the 95% confidence interval indicates a larger error than the mean of the multiple linear regression fit, but these estimates are still a factor of two to three times more accurate than Foster's or Schmidt's estimates. Additional test cases would probably reduce the size of these confidence intervals.

10.0 Speedup Ratio of Estimation

The proposed estimation technique, combining separate

models for net distribution and net segmentation produces accurate estimates 10^2 to 10^3 times faster than actually routing the boards, as shown in Figure 7. The actual speed up ratio is larger because the estimation technique directly provides the minimum number of routing layers, which would otherwise take several iterations of the routing algorithm. This comparison is shown in Figure 7.

Board Name	Run Time of Estimation	Run Time of Actual Routing	Speedup Ratio
bd1	15 sec.	4.5 hours	1100
bd2	14 sec.	4.6 hours	1200
bd3	15 sec.	4.5 hours	1100
db	13 sec.	1.1 hours	300
mmm	15 sec.	6.3 hours	1520
mmd	13 sec.	2.1 hours	600

Figure 7. Speedup Ratio of Estimation vs. Actual Routing Job

11.0 Conclusion

Combining net distribution with net segmentation results in a routing layer estimation model that is two to five times more accurate than previously reported estimation techniques. The estimation technique is also 10^2 to 10^3 times faster than per-

forming the actual routing. This results in a savings of design time while achieving lower cost boards. The authors wish to thank to Professor Rajeev Jain (UCLA) for his insightful discussions.

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Table 1: Net Segmentation Model Coefficients

Coefficient	Horizontal		Vertical	
	95% Confidence Interval	Mean	95% Confidence Interval	Mean
a0	(1.16, 7.02)	4.33	(-9.85, -2.01)	-5.93
a1	(-0.02, 0.01)	-0.01	(0.91, 0.12)	0.10
a2	(0.19, 0.81)	0.50	(0.57, 0.77)	0.67
a3	(1.39, 1.71)	1.55	(2.91, 3.28)	3.10
a4	(-0.26, 1.49)	0.61	(-3.12, -1.95)	-2.37
a5	(-0.41, 0.36)	-0.02	(-0.05, 0.26)	0.10

Table 2: Comparison of Estimation Techniques on Test Cases

	% Error		
	Foster's Algorithm	Schmidt's Model	Proposed Model
Avg. Max. Horizontal Wiring Dist. Value	19	16	7
Avg. Max. Vertical Wiring Dist. Value	32	21	3
Avg. # of Horizontal Routing Layers	41	16	0
Avg. # of Vertical Routing Layers	41	16	8
Avg. Total Horizontal Wirelength	21	45	7
Avg. Total Vertical Wirelength	31	33	5