A Digital Method For Testing Embedded Switched Capacitor Filters

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Abstract

The ever increasing integration of analogue and digital functions on the same IC has increased enormously the problem of testing these complex circuits. Many analogue functions are implemented using switched capacitor techniques whose inputs and outputs may be difficult to access. This paper describes a built in test technique for testing embedded SC filters. The technique proposed is called M–sequence testing and has the advantage that much of the test hardware required can be realised from registers in the digital part of the circuit.

1. Introduction

Recent advances in process technology have allowed the fabrication of both analogue and digital functions on the same IC. These mixed function circuits are finding wide use in applications ranging from communication systems to medical electronics. Some of these applications require a degree of programmability in the analogue functions. This is achieved through the use of switched capacitor (SC) techniques.

However SC circuits are more prone to failure than normal RC circuits, since the additional FET switches used to replace certain resistor/capacitor functions have more failure modes.

In the past with mixed analogue/digital circuits, there was a tendency to place the analogue part close to the pads, for easy access during testing. However with present day circuit densities this is not always practical since problems such as power supply coupling and substrate coupling limits the freedom the designer has when laying out functions. As a result a layout may occur where the analogue function is embedded with little or no direct access for testing purposes. Although several methods [1–4] have been proposed for testing embedded analogue functions, further work is required particularly with respect to switched capacitor and switched current circuits.

2. M–Sequences – Theory

The M–Sequence test method is derived from the impulse response testing technique used in control theory (Towill [5]), in which a periodic noise signal is applied to a system and the impulse response is subsequently generated using the Wiener–Hopf equation shown in equation (1) where Φ_{XX} is a unit impulse and Φ_{XY} is the impulse response of the system.

$$\Phi_{XY}(\tau) = \int_0^T h(\tau_1)\Phi_{XX}(\tau - \tau_1)d\tau_1 \qquad (1)$$

An M–sequence is a bipolar periodic noise sequence which can be generated from a linear feedback shift register (LFSR) contained in the digital circuitry Tsao[6].

2.1. M–Sequence Parameter Calculation

In order to obtain an acceptable impulse response from the circuit under test, the parameters of the M–sequence must match the circuit, in particular the pulse width and length of the M–sequence with the decay time of the circuit. Davies[7]

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describes the method of obtaining suitable M–sequence parameters from the Laplace transform of a control system. In the case of SC circuits, the Z–transform is used instead of the Laplace transform. As an example consider the calculation of the pulse width required for a 31 bit M–sequence applied to the SC filter shown in Figure 1 which has the following Z–transform:

$$\frac{Y[Z]}{X[Z]} = \frac{5.1 \ * \ 10^{-3} \ Z^{-1}}{1.0594 \ - \ 2.0542 \ Z^{-1} \ + \ Z^{-2}} \qquad (2)$$

The Inverse transfer function gives the calculated impulse response of the filter:

$$Y[nT] = [0.9715]^{n} \ * \ 0.078[sin \ \ 0.065n] \qquad (3)$$

(T = Sampling Period)

From equation (3) the impulse response decay time is calculated to be:

$$T_{decay} = 12.4ms$$

Therefore from Davies [7]:

$$N\Delta\tau = 12.4ms \qquad (4)$$
$$\Delta\tau = 12.4ms/31$$
$$\Delta\tau = 0.4ms$$

2.2. Impulse Response Generation

Figure 2 shows the impulse response generated from a simulated test circuit along with the impulse response calculated using equation (3). The generated response was obtained by applying the M–sequence to the SC filter and then correlating the output response with a version of the M–sequence delayed by 1Δτ, then 2Δτ up to 30 Δτ (where Δτ, equals the pulse width within the M–sequence).

For testing purposes the generated response compares favourably with the calculated response and can therefore be used as a ’Signature’ for the fault free state of the circuit.

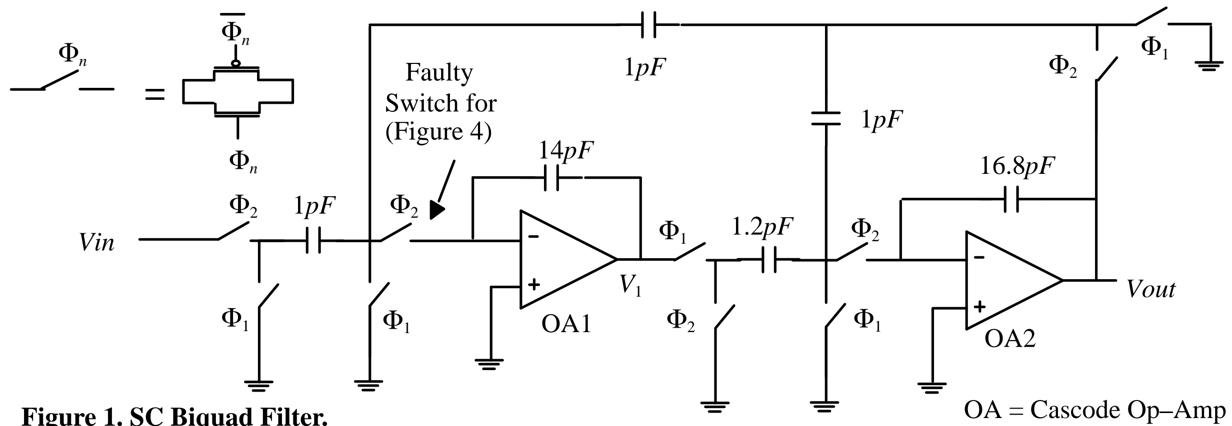
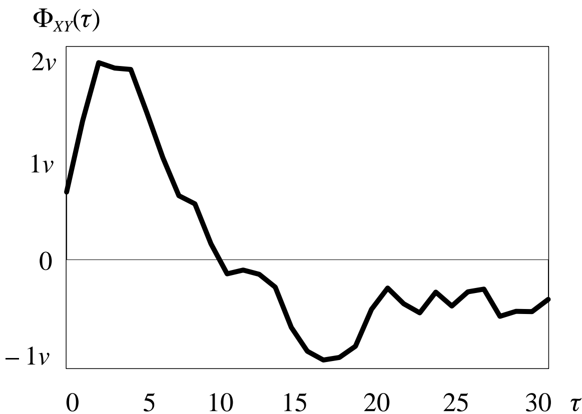


Figure 1. SC Biquad Filter.



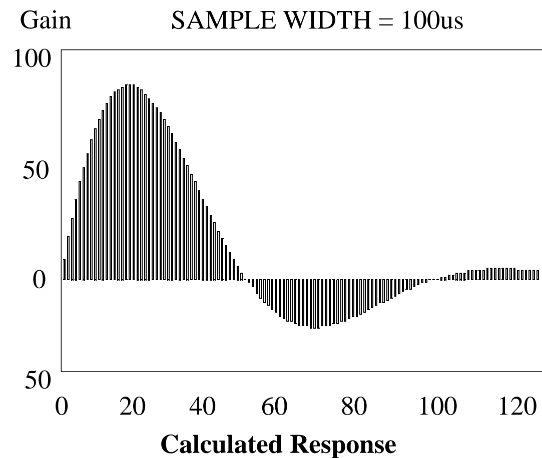


Figure 2. **Generated Response** **Calculated Response**

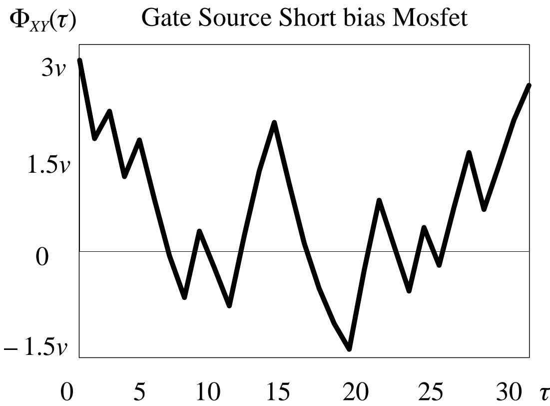
The fault detection capabilities of the technique were demonstrated using the now standard FET fault model [8] to simulate the effects of common faults such as drain/source opens and gate to drain/source shorts in the devices within each of the two Op–amps and also on the transmission gate switches of the filter. Each transistor in the circuit was replaced in turn with the FET fault model and a corresponding impulse response was generated. The faulty responses were then compared with the fault free response. Figure 3 shows the responses generated from two faults in the first Op–amp of the SC filter and Figure 4 shows the responses generated from two faults in one of the transmission gates.

Examination of all the responses showed that all the transmission gate faults and up to 85% of Op–Amp faults can be detected using this technique. However there are a number of faults which have no effect on the functionality of the Op–Amps and cannot be detected. Also other types of faults such as gate oxide shorts merely cause small voltage offsets in Op–Amps and have no effect on the overall response of the filter. However these types of faults do result in a change in power supply current. The next section discusses the possibility of using current mode M–sequence testing to generate impulse responses using the power supply current of each Op–Amp in the filter.

3. Current Mode M–Sequence Testing

If a resistive load is placed on the output of the filter and the current flowing from the power rail into the second Op–Amp (OA2) is examined it is seen to consist of the d.c bias currents of the Op–Amp and the current flowing through the output stage to the load. The output current will have the same pattern as the output voltage (Vout).

Hence if the current flowing into OA2 is copied via a current mirror and the d.c bias currents eliminated it can be used to generate the impulse response of the filter.



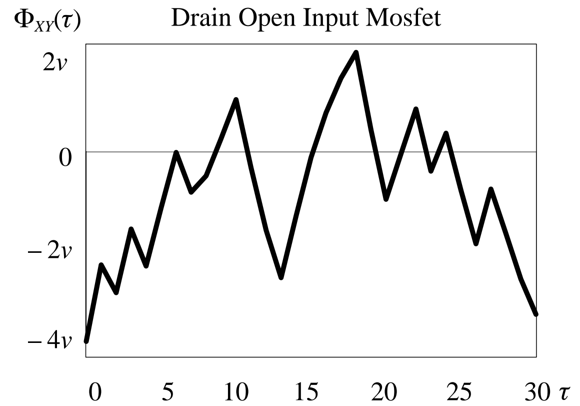
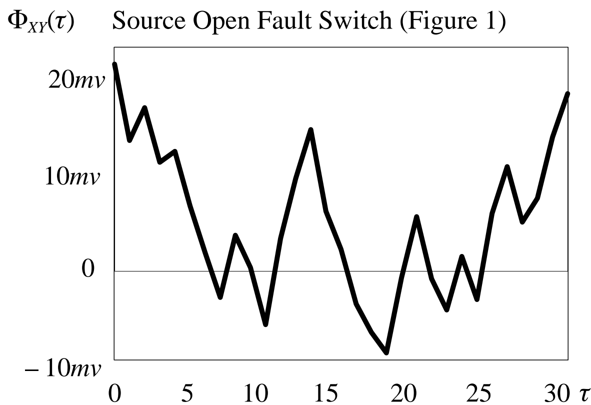


Figure 3. Impulse Responses with Faults in Op Amp 1.



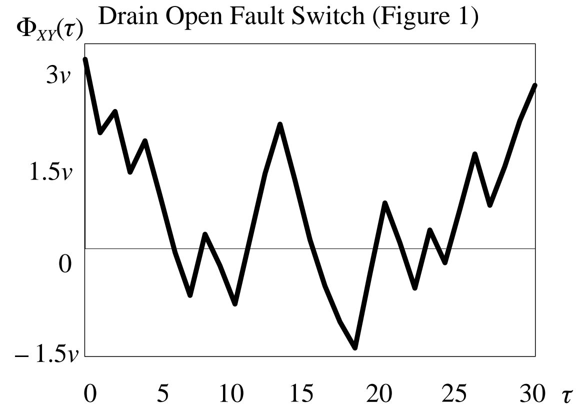


Figure 4. Impulse Responses with Transmission Gate Faults.

Furthermore if a resistive load is placed on the output of the first Op–Amp (OA1) the current which flows through the output stage will have the same pattern as the output voltage (V1). Since the SC filter can be considered to consist of two lossy integrators, an impulse response can be generated by copying the current flowing into OA1, eliminating the d.c bias currents and feeding the residual current signal into two switched current (SI) lossy integrators (Toumazou [9]) connected in a feedback path.

3.1 Test Circuit

Both impulse responses can be generated using the switched current circuit shown in Figure 5. The circuit consists of a SI filter made from two lossy integrators and one SI memory cell connected together in a chain. Each block contains a current mirror to copy the corresponding Op–Amp power rail current and also a NMOS current sink to eliminate the Op–Amp d.c bias currents.

The clock used in the SI circuitry can be taken from the SC biquad filter if it is delayed by 1/4τ (τ = clock period). The delay is necessary in order to stop large power rail current spikes which are caused by the transition of the biquad switches from affecting the bias currents in the SI circuitry.

When an impulse response is required from OA2 the SI filter block is disconnected. The SI memory cell is used to hold the current signal before it is converted into a voltage signal by the CMOS inverter. The voltage signal is then fed into the correlation circuit to generate the response of the filter.

The impulse response from OA1 is obtained by connecting the input of the SI memory cell to the output of the SI filter. The current signal copied from OA 1 is inverted and filtered in the SI filter block before being fed into the SI memory cell and converted into a voltage signal.

Figure 6 shows the impulse responses obtained from both Op–Amps. They are both similar to the responses in Figure 2 and can therefore be used as a fault free signature. Figure 7 shows the responses generated from the same Op–Amps containing a fault which could not be detected using the original M–sequence technique which was essentially a voltage measuring technique.

3.2 SI Test Circuit – Practical Considerations

The reliability of the test circuitry is an important factor regarding the acceptance of a new test methodology. The test circuitry is just as prone to failure as the circuit it is testing and hence needs to be tested as well.

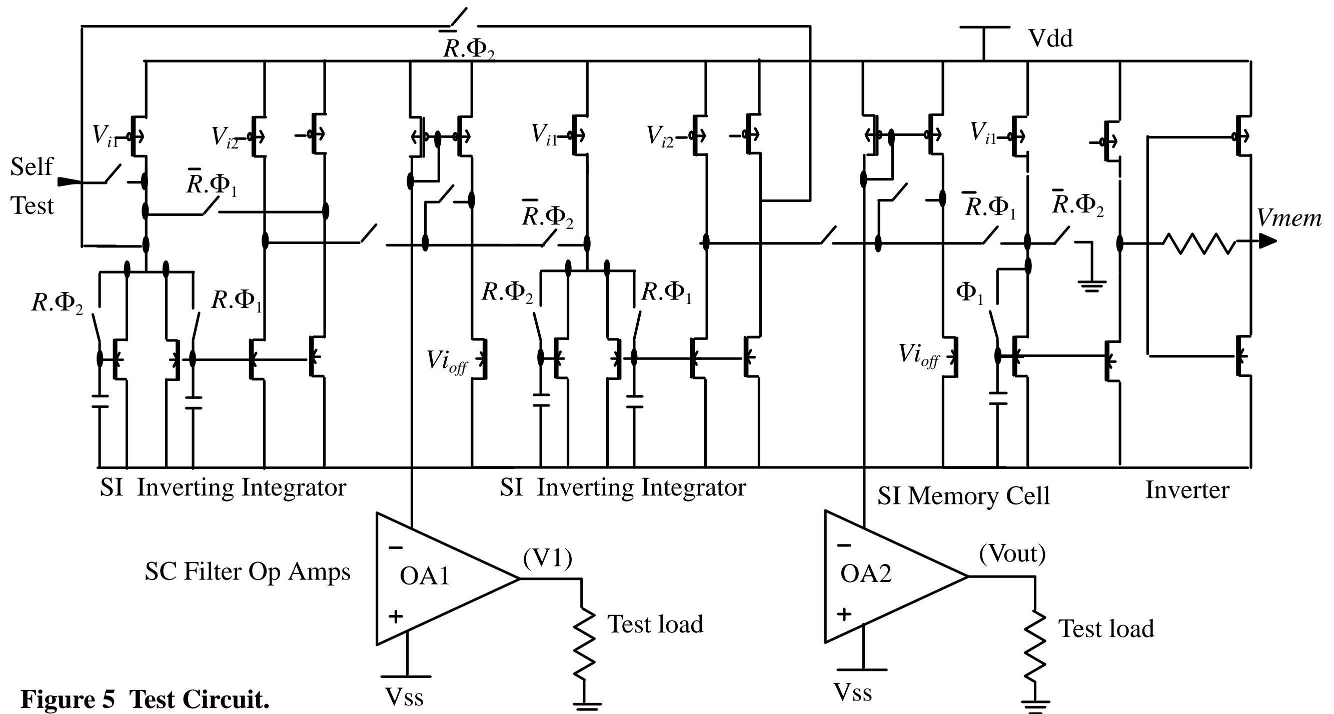


Figure 5 Test Circuit.

The M–sequence generation and correlation circuitry can be tested if the circuit under test is by-passed. The M–sequence will be autocorrelated and a ’unit impulse’ will be produced which denotes that the test circuitry is fault free.

The SI testing circuitry is basically a standard SI filter (Tomazou [10]). The application of a current mode M–sequence signal via a transconductance amplifier can yield the impulse response of the testing circuitry. This response can also be used as a fault free ’signature’ thus the technique is self testing.

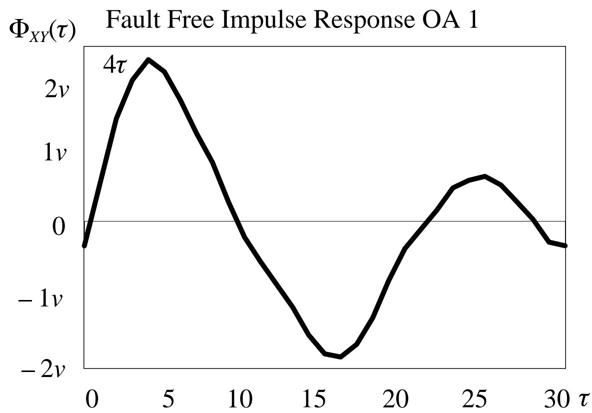
Presently SI technology is in the early stages of development. Problems such as charge injection, transistor mismatch and low signal swing has meant that the signal to noise ratio is much lower than SC filters especially at low frequencies. However, although the S/N ratio is quite poor the output is correlated so the noise has a minimal effect. Therefore although SI technology is not viable for low frequency applications in mixed mode ICs it can be used as part of the test circuit for this technique.

4. Complete Test Circuit

One of the main advantages of this technique is that the same testing circuitry can be used to test a number of SC filters. Varying the pulse width according to Section 2.1 can result in all of the SC filters under test yielding the same impulse response.

With reference to Figures 6 and 7 it is seen that the examination of the two points at delay values 0τ and 4τ are sufficient to detect if the circuit is faulty or not. Hence it is not necessary to generate the complete impulse response as outlined in Section 2.2, only the correlation points, in this instance at 0τ and 4τ are required. Figure 8 shows the block diagram for the implementation of the technique.

The reference M–sequence generated from the LFSR (Tsao[6]) is applied via an analogue multiplexer to the required SC filter under test. The SI testing circuit output is then correlated with either the same sequence (0τ) or the delayed sequence (4τ). The resultant response value (Φ_{XY}) is then compared with the fault free value using a window comparator.



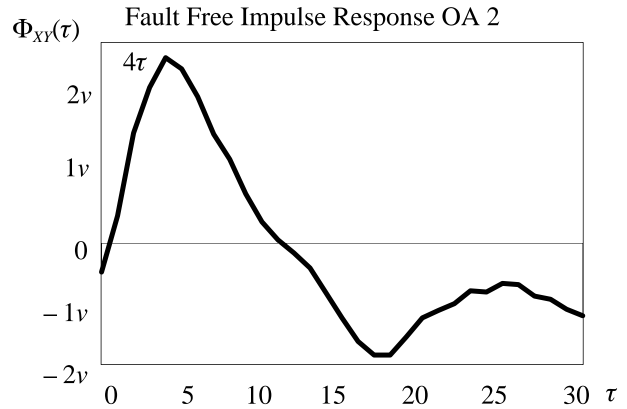
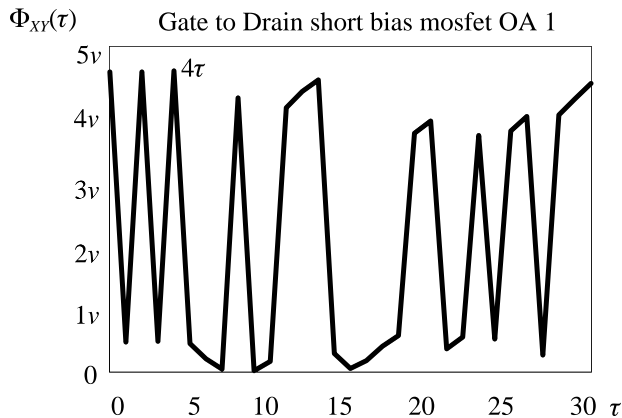


Figure 6. Fault Free Impulse Response Current Method.



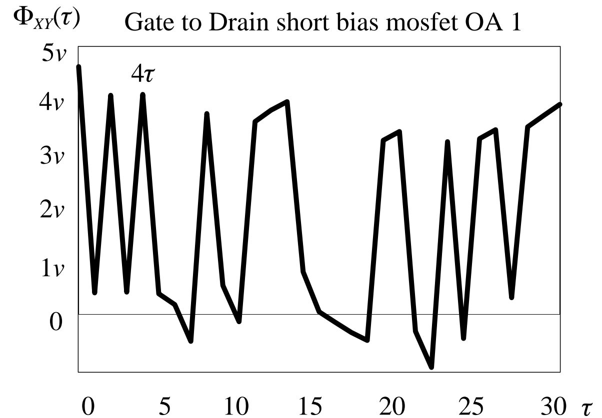


Figure 7. Faultly Impulse Responses Current Method.

A small digital controller integrated into the main digital circuit can be used to vary the M–sequence pulse width and control the SI testing circuit.The output from the comparator is digital hence it can be observed directly or integrated back into the digital test environment.

5. Conclusions

Two methods for testing SC filters within a digital testing environment have been presented. The voltage technique can be used in applications that require low power functional testing. The current monitoring method can be used in applications that require more thorough testing such as safety critical applications. The main advantages of these techniques are:

i) The techniques do not intrude into the actual design of the SC block.
ii) The M–Sequence and the delayed versions can be generated from existing digital hardware.
iii) The output from the testing circuitry is digital, hence no analogue output pins are required.
iv) The testing circuitry is self checking.

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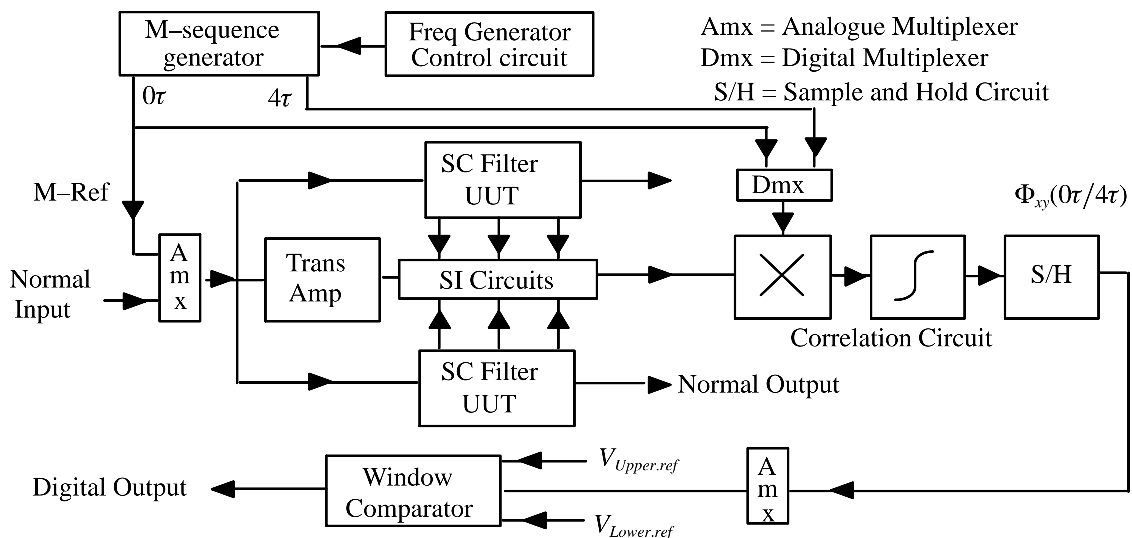

Figure 8. Full Circuit Implementation of Testing Technique.