New Approach in Gate-Level Glitch Modelling*

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Abstract

An enhanced gate-level glitch model for logic simulation is presented. This new approach can be used to enhance logic simulation accuracy and power estimation at little additional computation costs. The simulation algorithm is compatible with common event driven simulation models for glitch-free cases. Only if a possible glitch is detected the simulation is modified by our model. The model is based on common timing characterization data and a few additional constant values. The features of the model are enhanced scheduling of glitch events and prediction of glitch peak voltages, which are essential for precise power estimation.

1. Motivation

Modern IC-production lines offer deep submicron technologies. With the ever shrinking structures new possibilities arise for higher degree of functional integration, more complex applications in more handsome cases. For marketing, environmental and reliability reasons a low power consumption is gaining importance. For portable applications the time of battery operation is limited by its energy consumption. With the increasing power consumption of complete chips cooling problems arise which dramatically influence the packaging and its costs.

The power reduction of an application can be achieved by technology improvements, voltage scaling [1] and design decisions for low power [2]. Because of the high demands on lowering energy consumption all possibilities must be exploited.

Within design for low power the power consumption of a certain design solution needs to be evaluated. The power consumption of currently used static CMOS technologies is dominated by dynamic power consumption (except for very low-voltage supplies), i.e. the circuit activities need to be analysed. Precise simulation tools on circuit-level (like SPICE) can not handle the complexity of large circuits and huge number of possible patterns. For this reason the power calculation is based on circuit activity analysis at logic level. In order to precisely calculate energy consumption the logic node transitions must be examined carefully. It is important to note that multiple transitions within one clock cycle and glitches significantly (typically around 15-20% but in arithmetic units up to 65%[8]) influence power consumption [4,5]. This influence strongly depends on the architecture. Within this paper a glitch is defined as a pair of two or more colliding output waveforms which are so close together that the corresponding voltage waveform neither reaches V_{SS} nor V_{DD} in between (cf. fig. 1). A

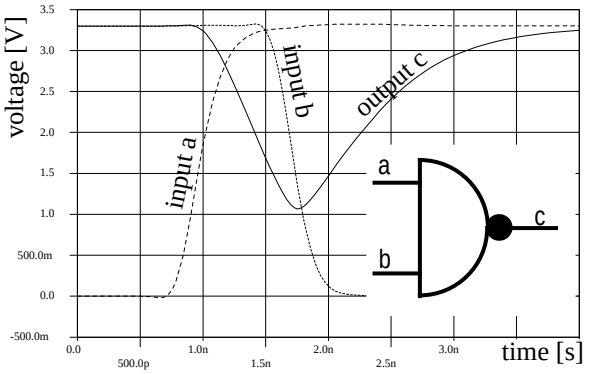

Figure 1: Example for a glitch at a NAND2-gate

glitch might even have a peak voltage which is less than the common logic threshold voltage (typically around 50% V_{DD}). A dynamic glitch initially starts at V_{SS} (V_{DD}) and ends at V_{DD} (V_{SS}). The energy consumption of a glitch is usually less than that of the underlying complete transitions and hence must be calculated differently. The new glitch

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model, which is the subject of this paper, includes the determination of essential data to consider glitches within the energy calculation.

In the next section the calculation of power consumption of static CMOS circuits on gate-level is explained. In section 3 the new glitch model is introduced and evaluated. A comparison with existing glitch models is investigated in section 4.

2. Power calculation of static CMOS

The average power consumption of a single CMOS gate can be divided into three parts:

$$P = P_{\text{leakage}} + P_{\text{short-circuit}} + P_{\text{Cap}}$$

The power consumption due to leakage currents is much smaller than the other two dynamic components and hence it is often neglected within power calculation. This is true except for very low voltage supplies and as a consequence for very low threshold voltages [2]. During switching a conducting path through the pullup- and pulldown-network of a gate is present and as a consequence a short-circuit current is occurring. The third component is the capacitive component which takes into account the capacitive loading of switched capacitors.

The calculation of the short-circuit power consumption is done by $\overline{I_{\text{short-circuit}}} \cdot V_{DD}$. The short-circuit current itself is hard to determine as it also depends on the capacitive current waveform [3,11].

Two complete transitions (one from 0→1 and one from 1→0) result in a capacitive energy consumption of $C_{\text{L}} \cdot V_{\text{DD}}^2$. The energy $1/2 \cdot C_{\text{L}} \cdot V_{\text{DD}}^2$ is associated with each transition. This later term does not strictly hold for single transitions because the voltage supply only delivers power when the capacity is charged (i.e. not when it is discharged). But in this case the assumption that the output capacity is lumped towards V_{SS} doesn't hold either [10]. However for average power estimation the typical operation is focused on and therefore the total number of transitions is quite high. I.e. that each rising transition (except maybe the last transition within the scope) is followed by a falling transition (and vice versa) so that the total energy consumption is calculated correctly.

If an incomplete transition occurs instead of a complete transition its energy consumption is:

$$\begin{aligned} E_{\text{Glitch}} &= 1/2 \cdot V_{\text{DD}} \cdot |Q_{\text{Cap}}| \\ &= 1/2 \cdot V_{\text{DD}} \cdot C_L \cdot |\Delta V| \end{aligned} \quad (1)$$

This equation also holds for complete transitions with $\Delta V = V_{DD}$. The capacitive power calculation is straight forward:

$$P_{Cap} = \frac{1}{2} \cdot V_{DD} \cdot C_L \cdot \lim_{T \to \infty} \frac{\sum_i |\Delta V_i|}{T} \quad (2)$$

The sum $\sum \Delta V_i$ can be obtained by logic simulation over a *sufficient* time interval [9] using the proposed glitch model. Equation 2 holds for all kind of glitches. As an example a dynamic glitch which consists of three ramps is illustrated in figure 2.

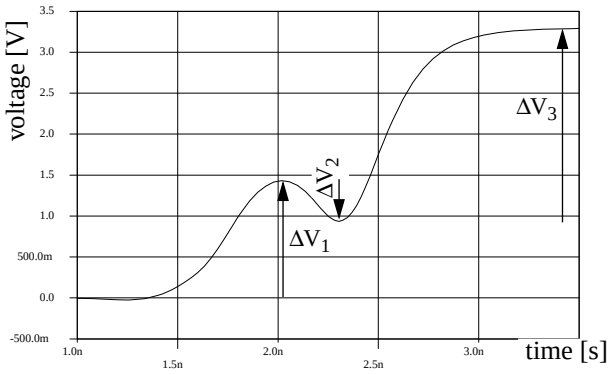


Figure 2: Example for a dynamic glitch

Modelling aspects of cell based static CMOS circuits have been dealt with in [10] in detail. However a glitch model was not included.

3. The proposed glitch model

It is often not considered [7], that for precise power estimation glitches may not be treated as two complete transitions but to predict the glitch peak voltage even on gate-level [6]. Using common logic simulation which is based on a transport or an inertial delay model does neither take glitch peak voltages nor the correct event scheduling in case of a glitch into account. To improve the event scheduling a dynamic delay model was proposed in [7] which unfortunately does not contain information about glitch peak voltages. In [6] a model to predict glitch peak voltages is proposed. This model lacks dynamic scheduling as in [7]. The proposed glitch model within this paper takes both into account: correct scheduling and prediction of glitch peak voltage and hence delivers better precision (cf. section 4).

The accurate prediction of glitches on gate-level relies on a good knowledge of delays. As the interconnections are tending to dominate the total load of a gate and therefore its delay, a backannotation step is gaining importance for glitch prediction. Generally the proposed model can be used for any timing model which contains slope information. But the precision of the simulation results is strongly influenced by the delay accuracy.

A glitch is typically generated by two colliding output ramps with opposite directions which are caused by two different input pins or a hazard at one input pin (i.e. a complete falling ramp followed by a complete rising ramp). This generated glitch might be propagated through consecutive gates. It is important to note that the output of the candidate gate through which the glitch might be propagated must be sensible to the input at which the glitch arrives. I.e. the probability of glitch propagation decreases with the number of gates in series (except for an inverter respectively EXOR chain). Therefore the precision requirements on the model are much higher for glitch generation and propagation at the first compared to the consecutive levels. It also should be emphasized that glitches tend to vanish or to be amplified to complete transitions during propagation which the model needs to take care of.

The basic idea is to represent a glitch by two or more linearly approximated ramps (cf. fig. 3). The ramps can be

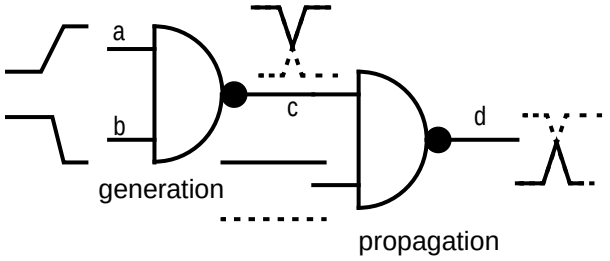
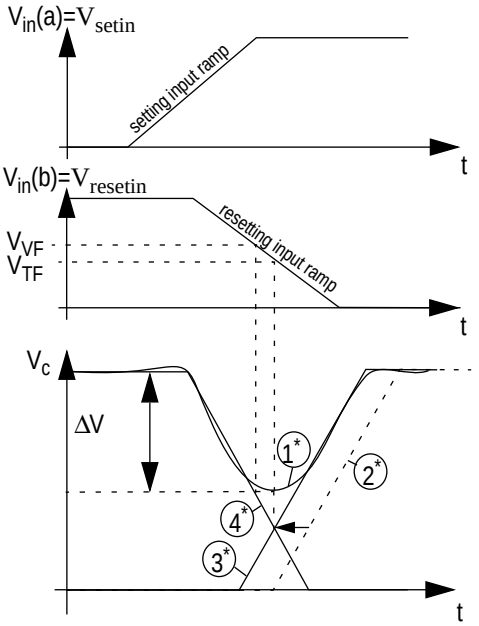


Figure 3: Representation of glitches by linear approximated ramps

easily derived from delay and slope information. A pair of a (colliding) setting and resetting ramp always represents a glitch or part of it (in case of more complex glitches). If a glitch is detected, the second ramp - defined as *resetting* ramp - is scheduled into the event queue differently than for a glitch free case. The reason for this is that the resetting ramp doesn't start from VDD (resp. VSS) for which the gate delay is characterised in the datasheets. The different scheduling of resetting glitch ramps has a significant impact on the propagation of the generated glitch.

The remaining question is how to schedule a resetting ramp and how to predict the glitch peak voltage. From the physical point of view, the voltage waveform's derivation is zero when the glitch peak is reached, i.e. no fanout capacity is either charged or discharged and the gate is in an *equilibrium* state. Hence at this instant the gate's dynamic operation point ($V_{resetin}$, V_{setin}, $V(1^*)$) (cf. fig. 4) is approximately equal to the respective static operation point, which leads to the idea to use static characteristics for glitch modelling. It is important to note, that static characteristics neither depend on a gate's input slope nor on its fanout load.

Within the new model four characteristic voltage values are introduced for each input-to-output-pin combination (cf. fig. 4):



1^* real glitch (from circuit-level simulation)

2^* non-colliding resetting output ramp (i.e. $V_{in}(a) = V_{DD}$)

3^* dynamically scheduled resetting output ramp 2^*

4^* non-colliding setting output ramp (i.e. $V_{in}(b) = V_{DD}$) - also refered to as V_{setout}

Figure 4: Glitch model and its characteristic voltages for a NAND2-gate (cf. fig. 3)

- V_{TF}: Voltage of falling input slope at time point when glitch peak is reached at output of stage
- V_{VF}: Voltage of falling input slope at time point when glitch peak voltage of linearly approximated non-colliding setting output ramp is reached
- V_{TR}: same as V_{TF} except that the input slope is rising
- V_{VR}: same as V_{VF} except that the input slope is rising

Each cell needs to be characterized with respect to these voltages.

The V_{TF}- and V_{TR}-values are used for scheduling the resetting ramp at the gate output. It is scheduled in such a way that it crosses the setting output ramp when the resetting input ramp reaches V_{TF} resp. V_{TR} and the *real glitch* (1^*) its maximum ΔV. The glitch is represented by the two ramps for possible glitch propagation.

The V_{VF}- and V_{VR}-values are used to predict the glitch peak voltage which is needed to calculate the corresponding glitch power consumption (cf. equation 2).

The effect, that the setting (non-colliding) output ramp (4^*) and the real glitch (1^*) diverge the more the resetting

input ramp takes control of the glitch, is modelled by taking different values for V_V (V_{VF} resp. V_{VR}) and V_T (V_{TF} resp. V_{TR}).

Due to the diverging waveforms of the real glitch and the non-colliding setting output ramp

- neither ($V_{resetin}$=V_V, V_{setin}, V_{setout}) at the instant when the resetting input ramp crosses V_V
- nor ($V_{resetin}$=V_T, V_{setin}, V_{setout}) at the instant when the resetting input ramp crosses V_T

exactly are the same as the triple of the real glitch reaching the equilibrium state. Hence the parameters do have a small dependency on the gate's output load and its input slope. This dependency has been analyzed by means of circuit-level simulation for various single stage gates.

As a typical example a NAND2-gate of an industrial 0.5µm-CMOS library (V_{DD} = 3.3V) is discussed here. It was analyzed within the testbench shown in fig. 5. An

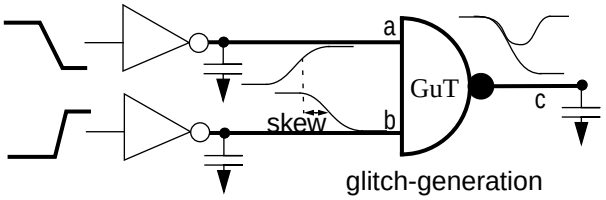


Figure 5: Investigation of characteristic voltage values

inverter is used to get realistic input slopes at the inputs A and B of the GuT (gate under test). The input slopes of a and b are modified by additional loads of the inverters. The capacitor between c and V_{SS} represents the GuT's load. For various combinations of capacities glitches with different peak voltages were generated by varying the input skew. The simulation results are shown in figure 6. The ordinate

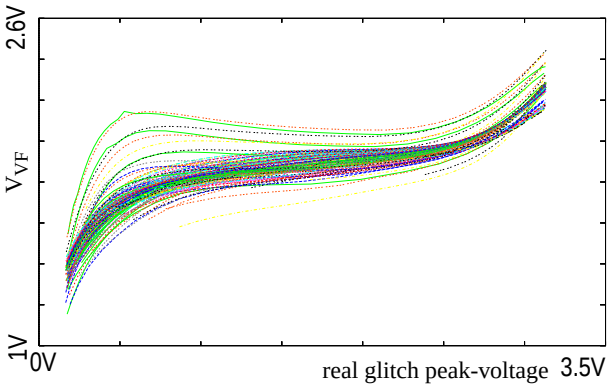


Figure 6: V_{VF} of a NAND2-gate for different circuit configurations

axis contains the values for V_{VF} and the coordinate axis the glitch peak voltage. The different curves correspond to a variety of different capacitor configurations. Small glitches result in smaller V_{VF}-values than bigger ones. This characteristic behaviour can be explained from the gate's static operation curve (V_c over V_b with V_a=V_{DD}). The impact of the setting input ramp (at a) is very low as it has reached a voltage level close to V_{DD} for most cases when the glitch reaches its peak. The few curves which are not within the *curve bundle* belong to very small loads at node c and slow setting input ramps of the GuT. For these cases the voltage of the setting input ramp is comparatively small when the glitch reaches its peak. However, the affected glitches result in very little power consumption and are no candidates for glitch propagation as the load is smaller than the smallest fanin capacity of a gate within the library.

For gate-level simulation purposes an approximation of the characteristic values (V_{VF}, V_{TF}, ...) by a constant average value is proposed. However, for improving the simulation precision the characteristic values' dependency on the glitch peak can be considered by calculating the glitch terms from the following equations:

($V_{resetin}(t)$, $V_{setout}(t)$) = ($V_V(V_{setout})$, V_{setout}) resp.

($V_{resetin}(t)$, $V_{setout}(t)$) = ($V_T(V_{setout})$, V_{setout}).

The simulation results of V_{TF} of the NAND2-gate are about 0.4V below those of V_{VF} and their characteristic curve waveforms look similar. The values of V_{VR} and V_{TR} for a NAND2-gate can only be determined by applying a hazard or a glitch to one input pin.

The glitching behaviour strongly depends on the characteristic non-linearity of each CMOS stage. Hence glitch simulation should be done stage by stage. It is important to note that for power estimation purposes of glitch-free cases transitions at stage output nodes which are internal nodes of a gate cannot necessarily be monitored at the gate output terminals. If a stage by stage simulation is not feasible the characteristic glitch values (V_{VF}, V_{TF}, ...) cannot be used as for single stage gates. On the cost of accuracy the proposed model can be adapted to multi stage gates by introducing an initial time-shift of the resetting input ramp.

4. Evaluation of proposed model

The proposed model is compared to the models presented in [6,7] with respect to circuit-level simulation by using a small benchmark circuit (cf. fig. 7 - the driving inverters for signal a and b are not shown). For the proposed model also non constant parameters V_V and V_T were analyzed (this model is referred to as proposed model enhanced). The following parameters were varied:

- skew: in steps of 60ps
- two different slopes at input a
- two different slopes at input b
- four different loads at c

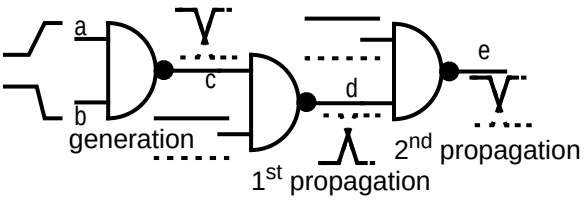


Figure 7: Benchmark circuit for evaluation of glitch model

- four different loads at d
- four different loads at e

For glitch analysis at node c six further slopes for both inputs a and b and four further loads at c were investigated.

Only cases which produce glitches for at least one of the models at the respective level (c, d and e) were considered. In total approximately 17800 different cases were examined. The delays and the slopes were directly determined by circuit-level simulation for each case (i.e. the focus is on glitch modelling and not on delay modelling of non-glitching transitions). The characteristic glitch parameters (V_{VF}, V_{TF},...) for the proposed model and the model presented in [6] were determined before.

Model [7] is basically not intended to predict glitch peak voltages. We extended the model by reading the voltage of the setting output ramp when the glitch peak is predicted. The setting output ramp is therefore constructed by the following two points (cf. fig. 8):

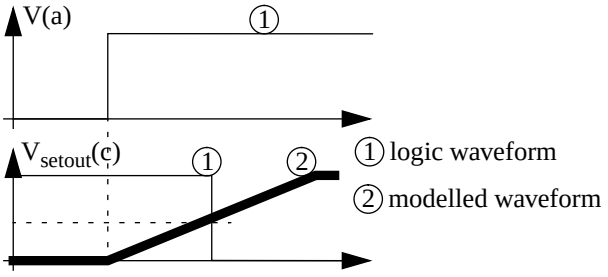


Figure 8: Ramp construction to make peak voltage estimation possible for [7]

- time when the output voltage equals $V_{DD}/2$ (which is a possible logic switching threshold),
- time when the setting input voltage equals $V_{DD}/2$ the setting output ramp starts from the initial voltage V_{SS} or V_{DD}.

For further details refer to [7,12].

In figures 9-11 the statistically analyzed difference between the simulation results achieved by circuit-level simulation and the gate-level model is shown (i.e., $value_{circuit\text{-}level} - value_{model}$). The presented values are:

- the glitch peak voltage ΔV error (fig. 9: mean value; fig. 10: standard deviation),
- the glitch peak time (fig. 11: mean value),
- the relative number of cases resulting in no transition within circuit-level simulation and a hazard (i.e. two complete transitions) for the logic model (fig. 12),
- the amount of glitches on circuit-level which are detected as glitches by the respective logic model (fig. 13).

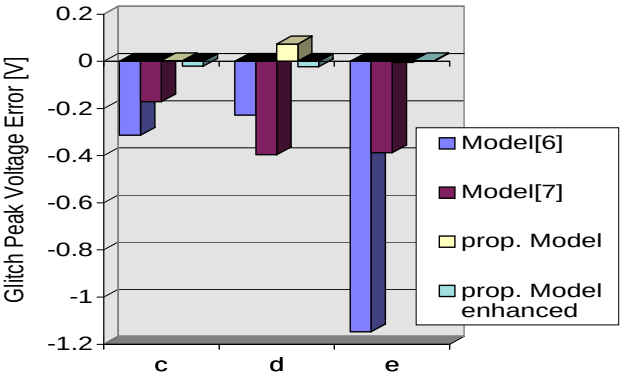


Figure 9: Mean value of glitch peak voltage error

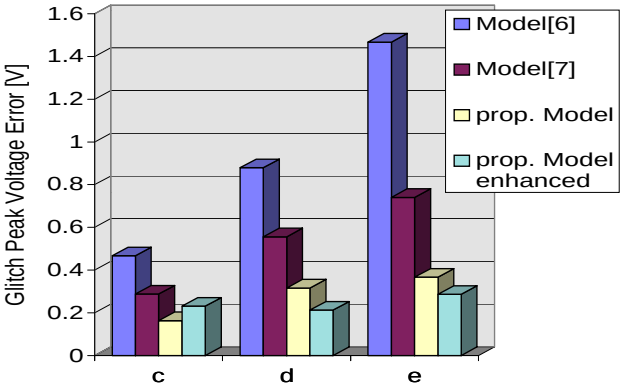


Figure 10: Standard deviation of glitch peak voltage error

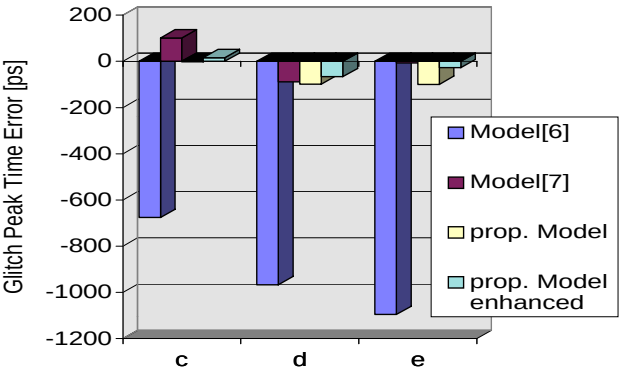


Figure 11: Mean value of glitch peak time error

Please note, that the results for the glitch peak voltage (fig. 9 and 10) were based on the cases where any of the models

or the circuit-level simulation result in a glitch. I.e. these figures can be used only for relative comparisons.

The missing dynamic scheduling methodology in model [6] clearly results in a pessimistic glitch estimation (i.e., the glitch peak voltage is significantly overestimated for d and e (fig. 9); glitches are less likely to be filtered during propagation (fig. 12); the glitch peak time is estimated too late for c, d and e (fig. 11)). Comparing the results of [7] and the proposed model with each other the peak voltage is estimated more precisely by the proposed model. The glitch peak time is estimated sufficiently accurate by both models. However the proposed model detects more of the glitches on circuit-level than model [7] does. By using non-

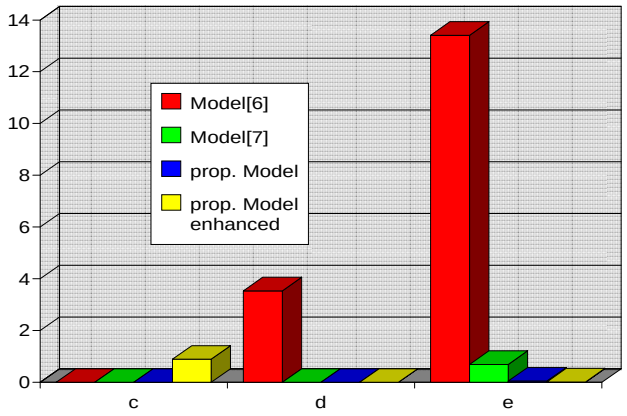


Figure 12: Relative amount of cases which result in no transition for circuit-level simulation and a hazard for the gate-level model in %

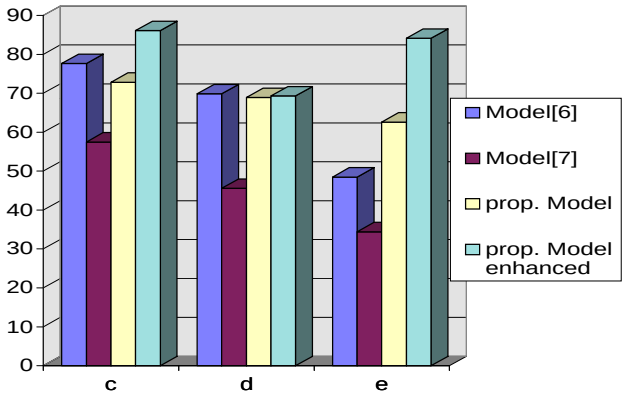


Figure 13: Relative amount of simulated glitches on circuit-level which are detected by the gate-level model in %

constant values for V_T and V_V the simulation accuracy on the one hand can be improved a little. On the other hand more characterization data is needed and the simulation performance will be decreased. The glitch parameters for the model [7] are fixed by the definition of the logic threshold voltages (here 50% VDD) and hence cannot be adjusted to a different glitching behaviour like for the model [6] and the proposed model.

5. Conclusions and future plans

Within this paper an attractive way to simulate glitches on gate-level - including accurate scheduling *and* determination of peak voltages - has been introduced. On the cost of only four additional characterization values per input-to-output pin combination of each stage the power simulation can be enhanced significantly. By the comparison with the approach of [6,7] significant progress was demonstrated.

This model is currently being integrated within the Leapfrog Simulator of Cadence. Additionally a stand alone simulator is under implementation for accurate power estimation.

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