A Top-Down Mixed-Signal Design Methodology Using a Mixed-Signal Simulator and Analog HDL

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Abstract

We have applied a mixed-signal simulator and AHDL to the top-down design of industrial ICs. We report the design process from the system-level down to gate/transistor-level modeling and simulation applied to a real circuit. We have verified the robustness and effectiveness of our approach which resulted in shorter design process cycles and higher rates of success.

1. Introduction

Advances in very large scale integration (VLSI) technology allow the implementation of large and complex circuits on a single chip. However, due to this complexity, it is impractical to simulate a full chip at the transistor level in SPICE[1]. Mixed-signal simulation and analog hardware description language (AHDL) enable a top-down design approach for today's large mixed-signal ICs and shorten design cycles[2][3].

In this paper we describe our approach to the mixed-signal top-down design methodology including behavioral modeling with AHDL, transistor-level implementation, simulation and model optimization at various levels of accuracy. We have applied this method to the design of more than ten commercial mixed-signal ICs with significant improvement of the design process. The effectiveness of the method is demonstrated on a hard disk drive read channel circuit containing A/D and D/A converters, a voltage-controlled oscillator and a gain-control amplifier.

The remainder of this paper is organized as follows. In section 2, the novel top-down design methodology is briefly introduced. Section 3 concerns our design process with a real circuit as an example. In Section 4, we discuss the effectiveness and some issues related to our approach from the designer's point of view. Concluding remarks and future work are presented in Section 5.

2 Top-down design methodology

Traditionally, analog circuit design has been done in a bottom-up fashion. One reason for this is the lack of a suitable modeling language for analog behavior. This has changed in the last few years with the introduction of several commercial simulators with AHDL capabilities.

Figure 1 depicts our mixed-signal top-down design environment[4]. At the system level, the designer describes the system behavior using a hardware description language such as verilog-HDL^{TM} or spectreHDL^{TM}. At this level, the designer verifies certain behavioral characteristics of the system and modifies the design as necessary. This early verification avoids the wasting of valuable design time and engineering resources during detailed circuit implementation. This is one of the greatest advantages of the top-down design. In the bottom-up approach, the designer does not verify system specifications until the full circuit is implemented at the transistor level. If some specifications cannot be met at the transistor level, the designer has to go back and change the system architecture, which can be a costly operation at that point.

Next, the functional blocks are translated into lower-level representations and analyzed. At this stage, the designer can choose an arbitrary abstraction level for each block. For example, the designer in charge of filter design can model the filter at the transistor level while other parts are modeled at the system level for faster simulation. This multilevel simulation allows high accuracy where needed while providing abstraction where possible. If some block is found to be inadequate, the

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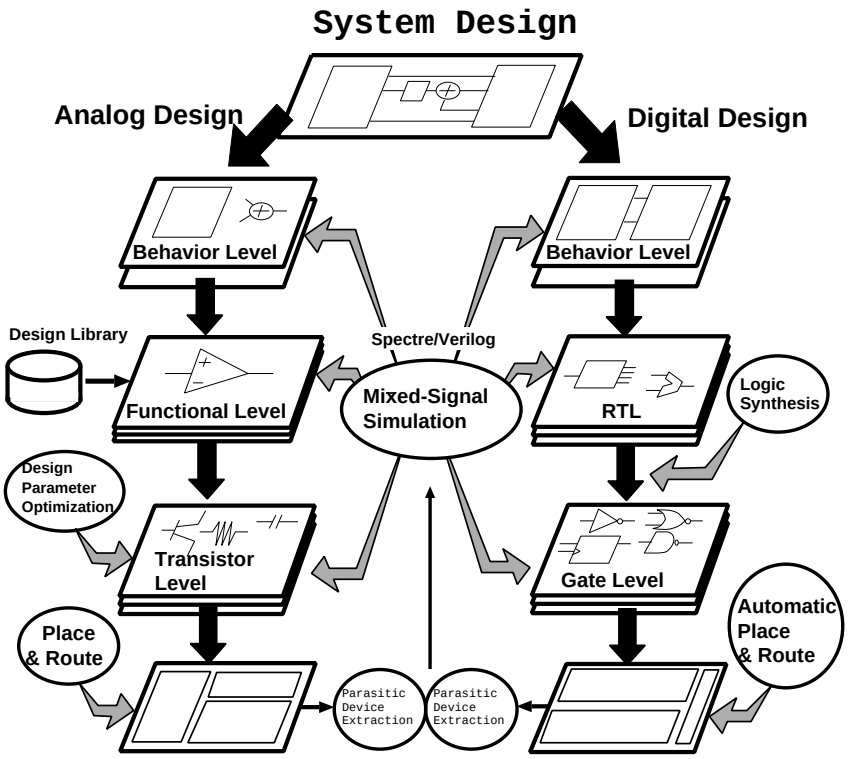

Figure 1. Top-down mixed-signal design environment

designer goes back to the upper level, tunes up the functional block specifications and resimulates the entire circuit. Finally, the gate/transistor-level design is verified by simulation and the necessary corrections are made. Hence, the top-down design methodology reduces simulation time and the number of design iterations needed through full chip verification.

3 Read channel IC design

Figure 2 represents a phase-locked-loop circuit for a hard disk read channel. Its input is a signal from a head amplifier. We model the signal as a piecewise linear voltage source. It is clamped by a gain control amplifier (GCA) and converted from analog to digital by an A/D converter. In the digital portion, the phase of the input signal and the output of an internal voltage-controlled oscillator (VCO) are compared. A control signal is fed back to the analog portion and the VCO output locks on to the input signal frequency.

3.1 System-level design

Initially, most blocks are expressed as ideal functions. For example, the behavior of the VCO is described as follows.

$$Mag * sin(2\pi * \int (Gain * V_{in} + FreeFreq)dt) + V_{offset}$$

where

$$\begin{aligned} Mag &: magnitude\ of\ VCO\ output \\ Gain &: VCO\ gain \\ V_{in} &: VCO\ control\ signal \\ FreeFreq &: VCO\ free-run\ frequency \\ V_{offset} &: output\ offset\ voltage \end{aligned}$$

Important components (VCO, A/D and D/A converters, etc) have been parameterized for easy adjustments later on. A loop filter is expressed in the s-domain which makes it easy to specify poles and zeros. At this stage, designing the ideal characteristics first frees the designer from details such as non-linearity. We model the filter as

$$F(s) = \frac{\tau_2 s + 1}{\tau_1 s},$$

where τ_1 and τ_2 are filter parameters. At this level, the total amount of AHDL codes was about 700 lines

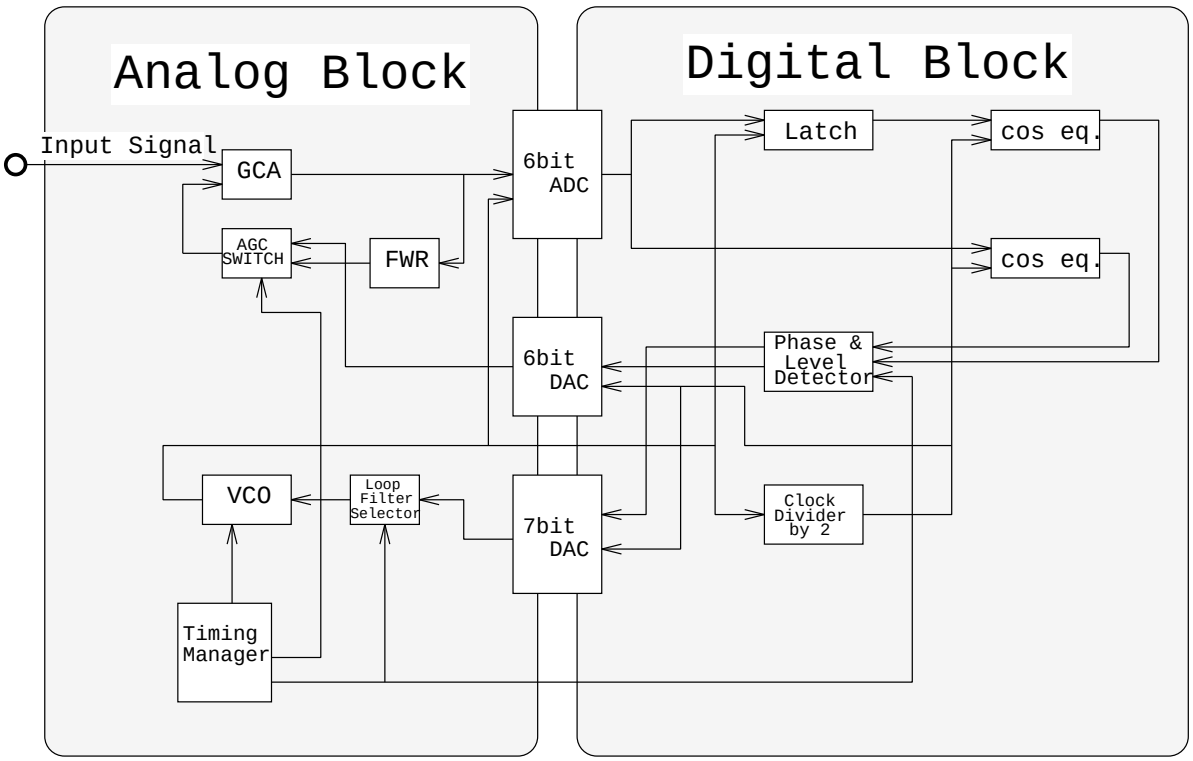

Figure 2. PLL circuit diagram

and that of verilog-HDL was about 1,500 lines. For the phase-locked-loop circuit, we simulated and verified the following.

- phase and gain tolerances
- switching behavior from a local loop to the entire loop
- lock-up time

Simulation results are shown in Figure 3. Total CPU times for the simulations at various abstraction levels are shown in Table 1. Since each simulation could be completed within a few minutes, we were able to examine a large number of test vectors. Some errors were detected by extensive simulation of the entire circuit for various input vectors. For example, some circuits behaved unexpectedly during PLL startup process. The designer in charge of the phase and level detector used theoretically generated data as a cosine equalizer output in his simulation. The data was valid from the beginning. However, since the real equalizer is three-tap FIR, its first two outputs are incorrect. The designer did not notice the condition until the system-level simulation detected the error. This kind of system debugging was possible only at this level.

Besides system-level debugging, we optimized circuit parameters such as the resolutions of the A/D, D/A converters and the filter parameters. Theoretically, these resolutions can be calculated manually, but it is hard to take analog and digital interactions into account due to propagation delays in the digital functions. Table 2 shows the initial value and final optimized value of the circuit parameters.

Table 1. Simulation times for multilevel simulation

Abstraction Level	Number of Elements		Simulation Time (s)
	Analog	Digital	
System-Level	20	20	341
Multilevel (GCA in Tr. level)	890	20	3523
Completely Analog	52000	0	$\gg$ 4000000 (estimated)

(on SparcStation 10/41
with 128MB Physical Memory)

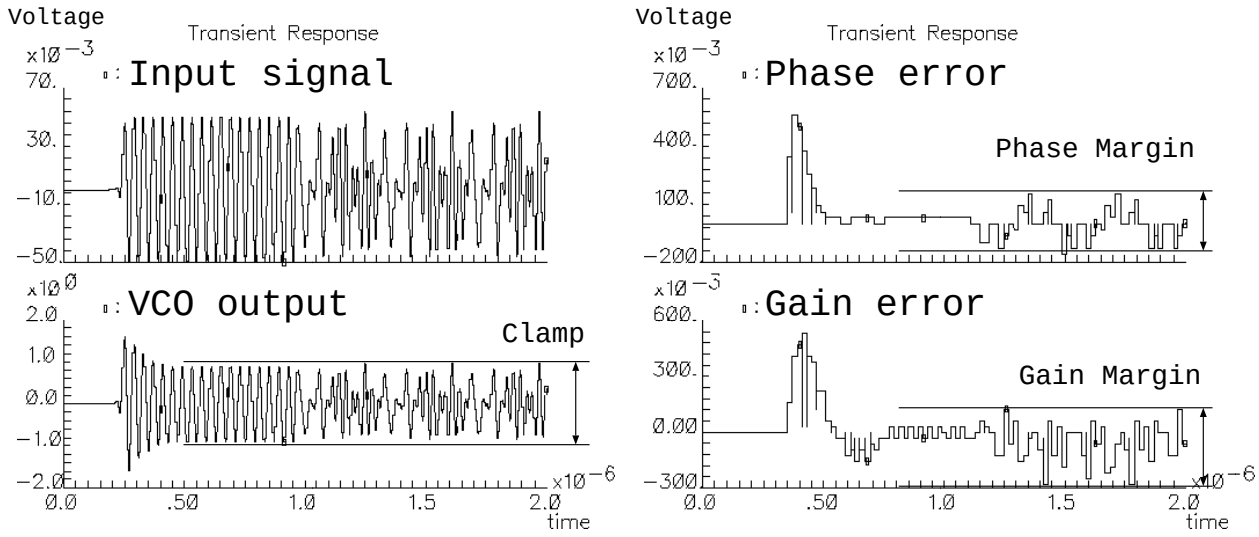

Figure 3. System-level simulation results

Table 2. Parameter optimization results

	Parameter	Initial Value	Final Value
Loop Filter	τ_1	2.0e-6	2.0e-6
	τ_2	3.0e-7	4.9e-7
ADC	resolution	5	6
DAC1	resolution	5	6
DAC2	resolution	5	7

3.2 Lower-level design

Once the system-level design is complete, the designer translates functional blocks into lower-level circuits. At this point, transistor-level simulation is necessary to verify the impact of nonideal effects such as nonlinearity and parasitics on circuit behavior. Digital gates can be synthesized from the register-transfer level automatically. On the other hand, analog circuit design is still a manual process. Circuit parameter optimization provides a practical alternative to analog circuit synthesis. In our design environment, some filters and amplifiers have been designed by the optimization technique[5]. For the other kinds of circuits the designer searches a design library for a block which is close to the required specification and makes minor modifications since it is time-consuming to design an analog block from scratch.

When translating analog behavioral models into lower-level circuits, one of the most crucial points is input/output signal levels. For digital blocks, the signal levels of the input/output characteristics are usually the highest and lowest voltages of the circuit for "True" and "False" respectively. On the other hand, analog input/output characteristics are spread over a wide range. The behavioral models should be created so as to reflect these points beforehand.

3.3 Design reuse

Once the transistor-level design of a block is complete, it is essential to fine tune the behavioral model to fit the transistor-level implementation for reuse in later design. Since reused blocks are simulated at the behavioral level by other designers, it is essential that the behavioral models are accurate and capture essential nonlinearities and second-order effects. Figure 4 shows the results of the initial behavioral model, the fine-tuned behavioral model and the actual response of the VCO at the transistor level. There is a good match between the results for the fine tuned behavioral model and the transistor level response.

4 Discussion

4.1 Productivity

In the top-down design process, there are two key factors that affect productivity. One is the effort and time required to develop models. The other is simulation speed. In model development, the designer should pay attention to the robustness and ease-of-use

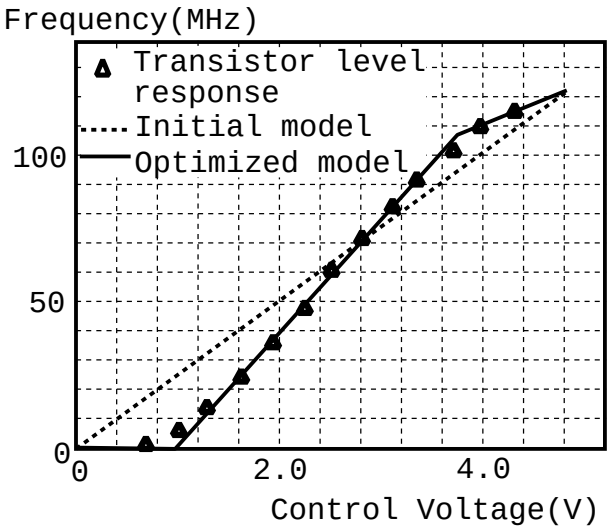

Figure 4. Optimization of behavioral modeling

of the models. To allow a smooth implementation of transistor-level circuits from behavioral models, it is important that parameters in behavioral models reflect real physical quantities in templates.

Simulation times for system-level and multilevel simulations are shown in Table 1. The figure for full chip simulation at the transistor level is estimated. It is clear from this table that the multilevel approach allows full chip verification in a reasonable time. We expect that turnaround time of large complex circuits to be reduced by as much as 50%. Faster simulation encourages designers to conduct a more thorough and extensive circuit verification.

4.2 AHDL issues

The top-down design process requires the designer to express his ideas mathematically. An in-depth understanding of the characteristics and limitations of the AHDL capability is thus required to devise accurate models for efficient simulation and good convergence. This poses a problem for most designers who are not used to using behavioral languages. To further ease the task of model development, a language-sensitive editor and a source-level AHDL debugger would be very useful. It is time-consuming and error-prone for a designer to create behavioral models from scratch. Therefore it is useful to provide parameterized skeletons (templates) of behavioral models which can be easily modified by the designer. Examples are parameterized A/D, D/A converters and general filter templates.

4.3 Mixed-signal simulation issues

For mixed-signal simulation, interface elements between analog and digital portions are inserted for domain conversion. In most cases these elements can be modeled in the simplified form of ideal voltage sources in order to speed up simulation. In some cases more accurate models are required to resolve interface nets accurately[6]. This requires again that the designer understands the impact of the interface models on the accuracy and properly selects the models.

5 Conclusions and future work

In this paper, we described the novel top-down mixed-signal design methodology and illustrated its effectiveness on a real circuit example. A key advantage of this method is the early verification of the system performance. This shortens the design time and reduces design iterations dramatically. Moreover, behavioral modeling significantly shortens the simulation time, allowing designers to conduct a more thorough verification at the full-chip level. We found that behavioral model templates and reusable model libraries are the keys to the acceptance of this methodology among designers. At Sony, this mixed-signal design environment has become indispensable for large complex systems.

The mixed-signal top-down design environment using AHDL is still immature, so many issues remain. We would like to investigate the incorporation of layout

parasitics in our design methodology including estimation in early design phases. Another area of interest is the further increase of our productivity in behavioral model generation.

6 Acknowledgements

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