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European Design Automation conference with
EURO-VHDL'96

PALEXPO
Sept. 16-20, 1996
Geneva, Switzerland

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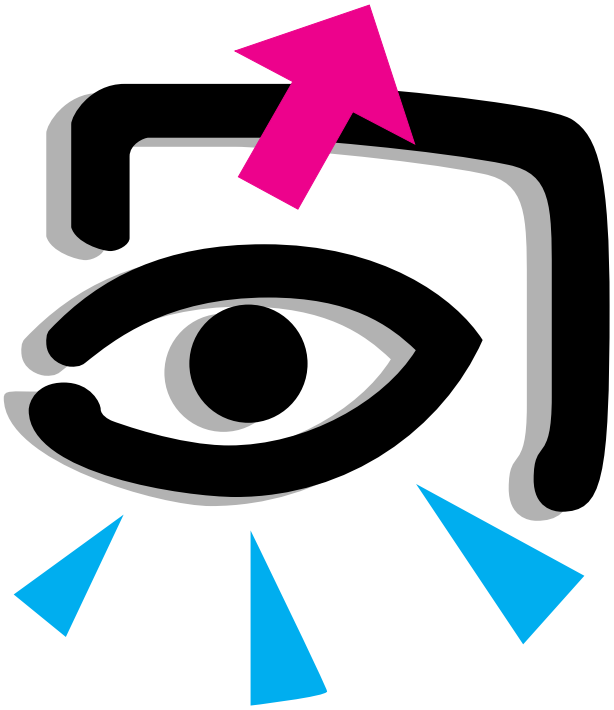

PALEXPO
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EURO-DAC'96

Proceedings

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EURO-DAC'96 — European Design Automation Conference with
EURO-VHDL'96 and Exhibition

Session D-01: Analog and Mixed Mode Simulation
Chair: Bernhard Klaassen, GMD, Sankt Augustin, Germany

The approaches presented in this session help to combine different levels of simulation: First, a hierarchical methodology for analogue behavioural modelling, followed by an approach combining timing and circuit simulation. The third paper presents a generalized coupling concept for analogue simulation.

Session D-02: Low Power Synthesis
Chair: Enrico Macii, Politecnico di Torino, Italy

This session presents two papers on techniques for low power analysis and synthesis. The first paper accounts for temporal and spatial correlations in estimating transition probabilities for sequential circuits. The second paper describes a state assignment technique for achieving low-power FSMs, given the input sequencies.

Session D-03: Design Experience
Chair: Klaus D. Mueller-Glaser, ITIV Universität Karlsruhe, Germany

Experiences in methodologies and tools used for the design of electronic control units in automotive and robotic applications are presented. Issues are specification, system level modelling and simulation, HW/SW tradeoffs, Fuzzy vs. PID-control, analog ASIC design, commercial tool usage.

Session D-04: Timing Modeling
Chair: Jacques Benkoski, EurEPIC Sarl, Gières, France

This session covers the evolving nature of the timing problems; what were previously second order effects such as glitches and interconnect must now be modeled. Asynchronous designs are also becoming more common and their timing problems mus be addressed as well.

Session D-05: Design Flow and Design Management
Chair: Ralph H.J.M. Otten, Delft University of Technology, The Netherlands

Starting from a novel approach for designing and implementing controllers targetted for structured data processing, design flows, design flow data management, design flow planning and control and design flow generation is discussed.

Session D-06: (Panel) What's Hot in Low Power Design?
Chair: Enrico Macii, Politecnico di Torino, Italy

For today's electronic devices low-power dissipation is desirable, and for some special applications, power consumption is a critical issue. An integrated framework for low power design of digital systems must provide the user with tools for low power synthesis at different levels of abstractions; in particular, low power consumption needs to be targeted at the system, architectural, logic and physical levels. Besides synthesis algorithms, the availability of tools for accurately estimating power consumption of systems at different stages of the design process is essential. This panel will investigate the progress that has been made in this area in the last few years. Both the academic and the industrial point of views will be illustrated and discussed by designers and scientists active in this field.

Panelists:
Jordi Cortadella , Universidad Politecnica Catalunya, Barcelona, Spain
Giovanni de Micheli, Stanford University, CA, USA
Massoud Pedram, University of Southern California, Los Angeles, CA, USA
Jan Rabaey, University of California at Berkeley, CA, USA
Rob Roy, NEC C&C Research Laboratory, Princeton, NJ, USA
Kees van Berkel, Philips Research Laboratories, Eindhoven, The Netherlands

Session D-07: Partitioning
Chair: Klaus Buchenrieder, Siemens AG, München, Germany

This session is introduced with an invited talk which gives a comprehensive overview of the state of the art in HW/SW partitioning. After that, two research papers present partitioning approaches based on combinatorial optimization methods.

Session D-08: Logic and FSM Synthesis
Chair: Utz Baitinger, IPVR Universität Stuttgart, Germany

The first paper incorporates sequential optimization into hierarchical synthesis. The second one describes a controller synthesis technique from regular expressions describing protocol-intensive applications. The third paper combines both behavioural and spectral domains in boolean matching for technology mapping.

Session D-09: BDD Optimization Techniques
Chair: Hans Eveking, Technische Universität Darmstadt, Germany

Two papers introduce compilation techniques and a new calculation method for boolean operations on OBDDs. In addition, decompositionand re-encoding procedures for the OBDD-based symbolic traversal of FSMs are presented.

Session D-10: Codesign Methodology and Cospecification
Chair: Klaus D. Müller-Glaser, ITIV Universität Karlsruhe, Germany

This session presents three papers on codesign approaches based on different specification formalisms. The first paper uses a combination of C, VHDL and a rules file, the second paper employs extended Statecharts, and the last paper is based on annotated task graphs.

Session D-11: System Level Design and Synthesis
Chair: Giovanni de Micheli, Stanford University, CA, USA

This session addresses system design issues for software and hardware. The first paper describes a technique for instructionset selection that can improve code quality for embedded DSPs. The second paper presents a system-level performance estimation technique that accounts for memories and pipelinded functional units. The last paper introduces packaging constraints into the system synthesis process by presenting a hierarchical behavioral partitioning algorithm.

Session D-12: New Aspects on Testing
Chair: Chair: Wilfried Daehn, SICAN GmbH, Hannover, Germany

This session addresses path delay fault testability, weighted random pattern testing, BIST, and the testable design of SC circuits.

Session D-13: Codesign Methodology and Cosimulation
Chair: Ahmed Amine Jerraya, TIMA/INPG, Grenoble Cedex, France

This session combines a paper on the cosimulation of mechatronic systems and three papers on codesign methodology. In the papers on methodology emphasis is given to design reuse aspects, life-cycle aspects, and the role of simulation in Hardware/Software Codesign.

Session D-14: (Joint Panel EURO-DAC and EURO-VHDL)
Which Formal Verification Technique is More Applicable in Industry Today: Equivalence Checking or Property Checking?
Chair: Luc Claesen, IMEC, Leuven, Belgium

Growing system integration and complexity currently require extreme attention towards design correctness. Formal verification methods have evolved over the last few year into industrial application. This panel will explore the potentials and difficulties for industrial adoption of formal verification in design flows.

Panelists:
Pierre Ragon, Philips TRT Communication Systems, Le Plessis Robinson, France
Michael Payer, Siemens, München, Germany
Frederic Rocheteau, SGS Thomson INMOS Ltd., Almondsbury, UK
Simon Read, COMPASS Design Automation, Rochester, MN, USA
Dominique Borrione, TIMA/INPG, Grenoble Cedex, France
Gerry Musgrave, Abstract Hardware Ltd. and Brunel University of West London, Uxbridge, UK

Session D-15: Key Technologies and CAD of Microsystems
Chair: Karl-Heinz Diener, Fraunhofer Gesellschaft — Institut für Integrierte Schaltungen, Dresden, Germany

The microsystem technology opens new ways for the integration of different sensors and actuators together with electronic components (mostly for information processing) on silicon. The inherent integration process is aimed at setting up flexible, adaptive, and intelligent systems intended to be applied to new products. The design of Microsystems requires to become familiar with both the dedicated technology for production and also the sophisticated CAD tools and systems. The goal of this session is to inform on what is feasible with key technologies for Microsystems, and how to design microsystems. That will be presented by two invited talks based on several examples of latest applications .

Session D-16: Asynchronous Synthesis and Storage Optimization
Chair: Jordi Cortadella, Universidad Politecnica Catalunya, Barcelona, Spain

This session contains two regular papers on asynchronous circuit synthesis and two short papers on techniques for storage optimization at the RT/logic and the behavioral level.

Session D-17: Modelling, Simulation of Microsystems and Multi Layer Routing in PCBs
Chair: Wolfgang Nebel, Carl-von-Ossietzky-Universität and OFFIS, Oldenburg, Germany

Because of their multi-disciplinary nature, the design of microsystems requires the using of CAD tools and systems. Modelling and simulation seem to be the crucial steps to coming up with right first designs. Two papers are addressed to that problem. Generally, the system integration realized by microsystems on silicon and PCBs, respectively, demands to pay most attention to achieving acceptable solutions of wiring the components necessary for creating systems. This problem will be tackled in the session, too.

Session D-18: Timing Issues in Synthesis
Chair: Kurt J. Antreich, TU München, Germany

This session contains papers describing issues at the behavioural, RTL and logic levels. The first paper describes a clock optimization technique for pipelined implementations of design behaviors. The second paper addresses the problem of false paths in delay estimation at the RT-level. The third paper describes a timing optimization technique at the logic level that employs improved redundancy addition and removal.

Session D-19: Physical Design for Deep Submicron
Chair: Tokinori Kozawa, Semiconductor Technology Academic Research Center, Tokyo, Japan

There are many restrictions to design sub-micron LSI. To solve this difficulties designer expect to have good tradeoffs by generic methods. An invited paper reviews the problem of deep submicron LSI design. The second paper gives an interactive floor planner based on the generic algorithm. The third paper presents a clock router taking the capacitance caused by parallel and cross segments.

Session D-20: Architectural Synthesis Techniques
Chair: Manfred Glesner, Technische Universität Darmstadt, Germany

This session contains three papers addressing different aspects of architectural synthesis. The first paper presents a combined approach for functional pipelining, component selection and scheduling. The second paper describes a low-power module assignment technique for pipelined design. The last paper uses self-checking as a requirement for scheduling in architectural synthesis.

Session D-21: (Panel) When do EDA Tools Hit the Submicron Wall?
Chair: Luke Collins, Electronic Times, London, UK

Panelists:
Jean-Marc Chateau, SGS Thomson Microelectronics, Grenoble Cedex, France
Moshe Steiner, Intel Israel Ltd., Haifa, Israel
Jacques Benkoski, EurEPIC, Gires, France
Franck Poirot, Compass Design Automation, Sophia Antipolis, France

Session D-22: CAD for Analog Circuit
Chair: Wolfram Glauert, University of Erlangen-Nürnberg, Erlangen, Germany

Since the constraints for analog LSI design are different from digital design, the conventional CAD for digital circuits cannot easily be applied to analog design. There are two papers charanging the difficulties of analog design. The first paper gives analog circuit partitioning dealing with analog specific constraints. The second paper presents and enumerative algorithm generating slicing placements.

Session V-01: Analysis Tools
Chair: Serafin Olcoz, TGI S.A., Madrid, Spain

The two papers of this session deal with an emergent topic: the analysis and estimation of the quality of VHDL descriptions. Quality covers the areas of testability, reusability, maintainability and portability. The measurements of these features will allow to VHDL designers to move towards and engineering approach to VHDL-based design.

Session V-02: Beyond VHDL
Chair: Wolfgang Ecker, Siemens AG, München, Germany

Born in 1985 as version 7.2, VHDL should be alive at least until 2015 considering the lifespan of military products. Or is it possible that the other parent of VHDL — namely IEEE, determines the lifespan of VHDL? This and other questions about the future of VHDL should be answered in this session.

Session V-03: (Panel) What Advantages Can We Expect from Object-Oriented Extensions to VHDL?
Chair: Jean-Michel Bergé, France Telecom CNET, Meylan Cedex, France

Object Oriented techniques have proven to be successful in software engineering. The temptation is therefore great to apply them to the hardware domain. The current version of VHDL does not support Object Oriented Modeling and several proposals for extending the language in this direction have been published. An IEEE study group has also been created on this topic. This panel will try to answer the question above from both the accademic and user point of views.

Panelists:
David L. Barton, intermetrics, Inc., McLean, VA, USA
Wolfgang Ecker, Siemens AG, München, Germany
Wolfgang Nebel, Carl-von-Ossietzky Universität and OFFIS, Oldenburg, Germany
Serafin Olcoz, TGI, Madrid, Spain
Gregory D. Peterson, Wright Laboratory, WPAFB, OH, USA

Session V-04: Fault Modeling and Design for Testability
Chair: Eugenio Villar, University de Cantabria, Santander, Spain

In this session, four papers addressing different aspects regarding the use of VHDL in fault modeling and desing for testability are included. The different techniques proposed aim to evaluate the design testability in the earlier stages of the design process thus reducing the design for testability costs of the whole design process.

Session V-05: Formal Methods
Chair: Werner Damm, Carl von Ossietzky Universität, Oldenburg, Germany

This session groups three complementary approaches towards the formal analysis of VHDL designs. The first paper provides a systematic approach allowing to characterize that subset of VHDL, whose behaviour can be faithfully abstracted to a synchronous finite-state machine. Suppose a design error has been detected, e.g. through model-checking, how do we then locate that part of the cirucuit responsible for the error? This question is answered in the second paper of this session w.r.t. a fault-model for gate-level designs claimed to be typical for design errors. Ideally, designs are correct by construction. A possible set up to systematically develop correct VHDL-code from logical specifications following the refinement paradigm is described in the last paper of this session.

Session V-06: Modeling Methodologies
Chair: Victor Berman, Cadence Design Systems Inc., Chelmsford, MA, USA

Session V-07: Synthesis
Chair: Ahmed Amine Jerraya, TIMA/INPG, Grenoble Cedex, France

This session deals with three important issues in synthesis with VHDL: Parallel controlled synthesis, timing constraints management, and extending VHDL subsets for synthesis.

Session V-08: System Level Design
Chair: Ronald Waxman, University of Virginia, Charlottesville, VA, USA

The underlying theme of this session is the power of VHDL to support many aspects of design at the highest levels of design abstraction. This range is exemplified by three papers. The range covers such diverse areas as asynchronous communication and hardware/software co-design, evaluation of fault tolerance and error detecting mechanisms, and specification modeling coupled with the design process.

Session V-09: VHDL and Mixed Signal Design
Chair: Alain Vachoux, Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland

This session begins with an invited paper in the IEEE VHDL 1076.1 standard proposal to extend VHDL to handle analog and mixed-signal systems. At that time, a ballotable language reference manual will be available. The IEEE ballot process is planned to start before the end of year 1996. The second paper proposes interesting guidelines to enhance the usability of VHDL 1076.1 to describe mixed-signal designs. The third paper is more tool oriented as it proposes a new intermediate format able to represent mixed-signal descriptions in a consistent way.

Session V-10: (Panel) The Open Forum Model
Chair: Victor Berman, Cadence Design Systems Inc., Chelmsford, MA, USA

†*Note: the author may be contacted for the full manuscript at:*

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Welcome

Welcome to EURO-DAC'96 with EURO-VHDL'96.

As we welcome you all to EURO-DAC'96 with EURO-VHDL'96 in Geneva, the fifth and premier event to support the European Electronic Design Automation Industry, we are realizing our objective of blending the latest scientific research with exhibits which display the best EDA-products worldwide with a User Forum for disseminating practical application experience.

The event gives the european professional greater access to the information needed to perform and excel in the fast pace world of Electronic Design.

As we enter the era of deep submicron design and complete systems on silicon new challenges are emerging for design automation if it is to stay in step with the rapid advances in implementation technology. These range from new modelling methods through more comprehensive analysis techniques; the merging of disparate design disciplines to new means to manage the volume of data and the design process. While designing at higher and higher levels of abstraction in order to deal with complexity is becoming the norm stronger links at all stages between specification and implementation are required in order to ensure finer geometries and faster clocking speeds from the manufactured devices.

But that is what makes our industry so exciting; over the whole range, from leading edge theory to user experience, the event will comprise panel sessions, tutorials, keynote talks and vendor sessions designed to stimulate lively discussion. At EURO-DAC '96 with EURO-VHDL '96 theory and practice ideally combine through the overall concept of conference and exhibition to progress the industry it serves.

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