Mixed-Signal Switching Noise Analysis Using Voronoi-Tessellated Substrate Macromodels

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***Abstract* - We present a new modeling technique for analyzing the impact of substrate-coupled switching noise in CMOS mixed-signal circuits. Lumped element RC substrate macromodels are efficiently generated from layout using Voronoi tessellation. The models retain the accuracy of previously proposed models, but contain orders of magnitude fewer circuit nodes, and are suitable for analyzing large-scale circuits. The modeling strategy has been verified using detailed device simulation, and applied to some mixed-A/D circuit examples.**

I. Introduction

As monolithic mixed-signal systems reach higher levels of integration, modeling and simulating the effects of fast switching transients have become increasingly important to the circuit design community. One critical issue involves the digital waveforms and their impact on the performance of sensitive analog circuitry on the same die. Noise coupling through the common chip substrate is a significant problem. Current injected across MOSFET source/drain junctions can propagate through the silicon and perturb the local substrate potential near the analog circuitry. The body effect modulates the threshold voltage of each transistor and, consequently, susceptible devices fail to perform as designed. The problem becomes more severe as clock rates increase, circuit features shrink, and applications demand greater precision from the analog circuitry.

Substrate modeling for circuit simulation was introduced in [1], where large 3-D resistive networks were formulated to study substrate coupling in low-power RAM cells. In [2], a so-called "single node" model was developed to investigate coupling in process technologies utilizing epitaxial silicon layers on heavily-doped substrates. While this approach produced less complex equivalent circuit models, the scheme was inappropriate for modeling substrate interactions in a lightly-doped bulk. In [3], a localized solution to Maxwell's equations based on a box integration technique was applied to the formulation of RC *mesh* networks representing interconnect lines and semiconductor substrates. This strategy was directly applicable to any substrate system, and in [4], was proposed as a method to study substrate-coupling in mixed-A/D circuits. In that work, the mesh-based approach was validated when results of a modeled substrate in a small example compared favorably to those obtained from device-level simulation. Later, in [5], a box-integrated substrate mesh yielded simulation results which were consistent with measurements obtained from the fabricated test circuit reported in [2]. Recently, the potential applications of substrate modeling have been extended beyond transient circuit simulation. In [6], coupling effects were included in the cost function of a simulated annealing - based power distribution synthesis system, and in [7], a method to plot substrate equipotentials derived from a perturbing noise source as a function of chip position was proposed as an aid for layout planning.

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All of the work presented to date is restricted to the generation of substrate models for small-scale analysis. In [1], [4], [5], and [7], rectangular mesh networks are generated by creating (*x*,*y*) grid boundaries at all relevant substrate feature edges as dictated by the fabrication photomasks. In all cases, *every* boundary line spans a cross-section of the *entire* layout plane. These strategies are not practical for large circuit-level analysis because the density of intersecting *x*- and *y*- boundaries can become very high even in chip areas where the density of substrate features is small. Since the density of intersecting grid lines equals the density of nodes in the derived network model, extraneous mesh nodes are introduced in substrate regions where they are not required to obtain acceptable simulation accuracy. For *any* raw, lumped element substrate macromodel, some measure must be taken to reduce the mesh complexity to achieve reasonable run times with existing simulators. This is typically accomplished by formulating "equivalent" networks, in which the internal nodes have been wholly or largely eliminated, while the circuit's port characteristics remain consistent with the original. Optimal intermediate network reduction algorithms for linear *mesh-like* RC circuits exhibit time complexities exceeding $O(N^{1.5})$ and storage requirements greater than $O(NlogN)$, where, for this application, N is the number of circuit nodes in the generated mesh [8]. For realistic circuits, N can grow so large that network reduction using conventional workstations becomes impossible. For this reason, it is of great advantage to constrain the size of the *original* mesh by adopting new methods of model generation.

We present a new modeling strategy which significantly reduces the computational complexity of substrate-coupled switching noise analysis by addressing the problem at the layout extraction / macromodel generation level. For efficient network reduction, what is really required is a grid which automatically adjusts itself to the local density of substrate features as dictated by the layout specification. To this end, we demonstrate a modeling technique based on a geometric construct called the Voronoi diagram and its dual, the Delaunay triangulation. No circuit nodes are introduced in the mesh regions where they are not required for simulation accuracy, and the nodal topologies of the resulting grids efficiently conform to the circuit layouts they represent. The models retain the accuracy of previously developed models but contain orders of magnitude fewer circuit nodes, thus reducing the burden imposed on the intermediate network reduction algorithms. Due to the superlinear complexity of these algorithms, the new approach provides mesh reduction speedups that are even greater than the node count ratio, and which continue to improve as circuit sizes increase.

II. Substrate Model Generation

In practice, layout methodologies are unpredictable. Most real chips contain areas of intricate complexity surrounded by comparatively large regions with little structural detail. In cell-based designs, for example, large chip areas contain no active devices but are dedicated to routing channels. *Rectangular* gridding methods for substrate model generation overpartition these regions of the substrate because locally dense mask features cause grid boundary crowding in other regions of the chip where it is completely unnecessary. In this section, a new substrate discretization based on a proven geometric formulation is shown to address this problem directly. The

configuration of the model's external nodes conforms *exactly* to the substrate features and MOSFETs specified by the layout data, and no nodes are added to substrate regions where they are not required. The derived nodal topology and doping profile information are subsequently combined to determine the branch circuit elements which interconnect the nodes of the equivalent circuit network.

A. Model Configuration

The modeling procedure yields a 3-D mesh of nodes with linear branch circuit elements. Layout data defines the mesh topology for every (*x*,*y*) *nodeplane*. Multiple (*x*,*y*) nodeplanes are then stacked and interconnected to extend the mesh in the *z*-direction (i.e., perpendicular to the substrate). The mesh is electrically connected to the active circuit at the top nodeplane. Nodes which are shared by both the mesh and the active circuit are the macromodel *ports*. Generally speaking, these are power supply nodes used to make ohmic contact to the substrate plus all of the MOSFET substrate terminals.

Let us first consider only the top (*x*,*y*) node plane, and its topological dependence on the extracted layout data. Underlying nodeplanes will subsequently acquire the same topology. For substrate modeling, relevant layout features include MOSFETs, wells, ohmic tie-downs, and guard diffusions. These features are represented by polygons derived from the layout specification. Each mesh node associated with a MOSFET substrate terminal or a substrate contact is called a *site*. Initially, the substrate feature polygons are converted to appropriate *internal point representations* — sites or groups of sites which are distributed in the polygons' interiors. At least one site is generated for each channel region or contact polygon, but large or irregularly-shaped polygons are represented by several sites. Additional sites are created near well boundaries, in large areas devoid of substrate features, and at the edges of the layout bounding box. Collectively, the generated sites comprise a distribution of *N* points in the (*x*,*y*) plane. With the exception of *fill sites* (i.e., those deliberately added in regions where site density is sparse), the site positions are derived entirely from the layout data.

B. Voronoi Tessellation

To significantly reduce the complexity of the formulated circuit network, we employ a geometric procedure called *Voronoi tessellation*. The *N* site locations can be used to define a planar, non-rectangular grid which enables the formulation of a substrate mesh containing far fewer nodes than previously published methods. The tessellation assigns a convex polygon to each site that spans the region of the plane which is nearer to the enclosed site than to any other site. The *N* polygons partition the plane into an *N*-region convex net called the *Voronoi diagram*; each region is called a *Voronoi polygon*. Theoretically, the tessellation extends to infinity, but the Voronoi polygons for convex hull sites (those adjacent to the layout boundaries) are truncated at the layout bounding box. Fig. 1a shows the Voronoi diagram for a random collection of 20 sites.

Voronoi tessellations possess a number of unique, interesting properties. In our case, the most important of these involves the straight-line dual of the Voronoi diagram, called the *Delaunay triangulation*. It is derived by joining each pair of data sites that share a common Voronoi polygon boundary. The edges of the Voronoi polygons are the *perpendicular* bisectors of the Delaunay triangle edges joining neighboring sites. This property will prove useful when formulating the branch circuit elements which interconnect the sites. The two geometric constructions form a mathematical dual because one can be completely deduced from the other — no extra information or computation is required. Fig. 1b shows the Delaunay triangulation for the 20-site example

Optimal algorithms for Voronoi tessellation have a worst-case time complexity of $O(NlogN)$ [9]. Although many proven algorithms

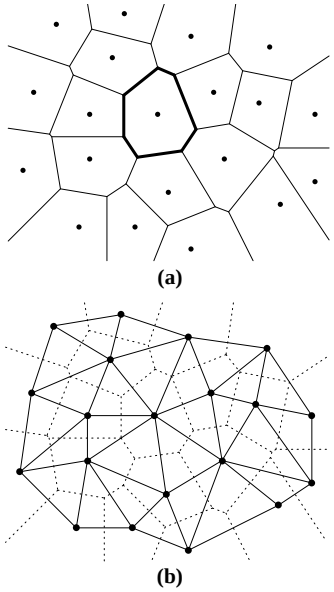


Fig. 1 (a) A Voronoi diagram and a constituent Voronoi polygon. **(b)** The Delaunay triangulation of the sites in (a).

meet this objective, we employ the *plane sweep* algorithm proposed by Fortune [10]. In terms of time and storage complexities, the algorithm is optimal. In addition, it can be efficiently integrated with the scanline algorithm we utilize to generate tessellation sites from layout data in the first place.

C. Model Derivation

In the rectangular gridding strategies described in previous work, mesh circuit elements were formulated based on geometric considerations and the box integration method utilized in [3]. In our approach, we consider individual Voronoi polygons and the *half* Delaunay triangle edges they enclose in order to derive the values of the linear circuit elements which comprise the mesh. First, a tile thickness, *t*, is assigned to each Voronoi polygon. The enclosed volume represents the region of silicon surrounding a Voronoi site. Each site becomes an electrical node in the macromodel mesh. A "Voronoi tile" and the associated triangulation edges are shown in Fig. 2.

We make two *a priori* assumptions regarding the electrical properties of a single Voronoi tile. First, the instantaneous value of the electric field, $\hat{E}$, is uniform inside the tile. Model accuracy will be compromised if the tessellation yields Voronoi polygons which are arbitrarily large. For this reason, fill sites are added to the plane in regions where the density of sites is known to be small. Secondly, the conductivity, σ, is assumed constant inside the tile volume. This

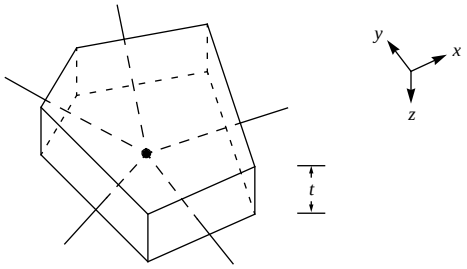


Fig. 2 A Voronoi tile enclosing a tessellation site. The segments of the Delaunay Triangulation are normal to the tile edges.

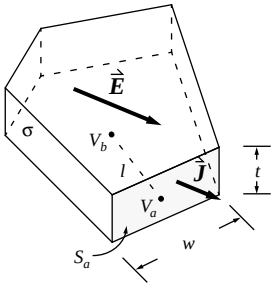


Fig. 3 A Voronoi tile used to formulate the substrate resistance. The tile conductivity, σ, is constant, and the electric field, $\vec{E}$, is uniform.

constrains the tile thickness, *t*, which must be chosen so that dopant concentrations inside the tile can be safely modeled by a single, mean value. The use of fill sites is described in Section IV. Details regarding the selection of *t* are presented later in this section.

Fig. 3 illustrates a Voronoi tile and one of the Delaunay half-edges associated with its site. Our objective is to compute the value of a resistor which models the current flow across the shaded tile face. We define V_b as the potential at the Voronoi site. V_a is the potential at the point where the triangulation intersects the tile edge. Then

$$V_b - V_a = \int_a^b \vec{E} \cdot \vec{dl} \tag{1}$$

where the line integral is performed along the Delaunay half-edge, *l*. Similarly, the tile face current can be computed by

$$I = \int_{S_a} \vec{J} \cdot \vec{ds} \tag{2}$$

where S_a represents the surface of the tile face. Since $\vec{J} = \sigma\vec{E}$,

$$R = \frac{V_b - V_a}{I} = \frac{\int_a^b \vec{E} \cdot \vec{dl}}{\sigma \int_{S_a} \vec{E} \cdot \vec{ds}} \tag{3}$$

The triangulation edge is perpendicular to the tile face, and (3) can be simplified to

$$R = \frac{l}{\sigma t w} = \frac{l}{\sigma A} \tag{4}$$

This technique yields the numerical value for the branch resistor between a site and the tile edge shared by an adjacent site in the (*x*,*y*) nodeplane. *l* is one-half the length of the Delaunay triangulation edge, and *A* is the area of the bisecting tile face. Mesh node-to-node resistor values for neighboring sites are thus determined by summing the two resistors associated with each Delaunay edge. For modeling the resistance *between* planes (i.e., when nodeplanes are stacked), (4) is applicable if *l* denotes the inter-plane spacing and *A* is the area of the Voronoi polygon. As a practical consideration, this approach yields exactly the same result as the box integration method if the Voronoi sites are distributed on a uniform grid.

It has been shown in [6] that the intrinsic bulk substrate capacitance has an inconsequential effect on the electrical behavior of the mesh at normal operating frequencies (i.e., up to a few GHz). Nevertheless, for CMOS circuits, mesh capacitors are required at well junctions to model the non-negligible depletion capacitance. For this reason, sites are deliberately introduced close to the well edges, and are created in pairs on opposite sides of the well boundaries. We call them *straddle sites*. As with the mesh resistors, the Delaunay triangulation is used to determine the placement of mesh capacitors. By design, the Delaunay edges between neighboring straddle sites have lengths which are approximately equal to the well junction depletion widths. Proper straddle site placement guarantees that the Delaunay edges are perpendicular to the well edges, thus simplifying the computation of the capacitor values.

The well depletion-layer capacitance is determined using the abrupt pn-junction approximation, and the nominal well / substrate reverse-bias voltage *V*, where

$$C = A\left(\frac{\varepsilon_{Si} q}{2} \frac{N_A N_D}{N_A + N_D}\right)^{1/2} (\phi_0 - V)^{-1/2} \tag{5}$$

In this equation, *A* is the tile face cross-sectional area for (*x*,*y*) branch elements, or the Voronoi polygon area for inter-plane capacitors. N_A and N_D are the junction mean impurity concentrations and ϕ_0 is the built-in potential.

Through σ in (4) and ϕ_0, N_A, and N_D in (5), the branch element values depend on the localized substrate impurity concentration which, for a given (*x*,*y*) coordinate, can vary continuously between the chip surface and the well junction depth(s). This region is discretized into *n* "slices" so that *n* "shallow" nodeplanes are used. Impurity profiles are modeled as stepwise-constant functions. The mean doping level, N_{mean}, for each slice is adjusted so that the integrated impurity concentration is equal for both the gaussian distribution and its stepwise-constant equivalent, i.e.,

$$\int_{z_1}^{z_2} N(z)\, dz = N_{mean}(z_2 - z_1) \tag{6}$$

$N(z)$ is assumed gaussian so that $N(z) = N_0 \exp\left(-(z/Z_c)^2\right)$. N_0 is the concentration at $z = 0$, and Z_c is the profile characteristic length, which can be expressed in terms of the bulk substrate doping concentration, N_{sub}, and the junction depth, Z_j, as:

$$Z_c = Z_j / \sqrt{\ln N_0 / N_{sub}} \tag{7}$$

Solving for the slice mean doping level yields

$$N_{mean} = \frac{\sqrt{\pi} N_0 Z_c}{2(z_2 - z_1)} \left[erf(z_2/Z_c) - erf(z_1/Z_c) \right] \tag{8}$$

The quantity (z_2 - z_1) in (6) corresponds to the tile thickness, *t*. If *t* is too large, the mean doping approximation can limit the model accuracy. For $z \le Z_j$, we constrain *t* so that the ratio of maximum to minimum doping concentrations within a slice does not exceed the factor *k*. Since the gaussian profiles are steepest at $z = Z_j$, this means that

$$N(z = Z_j - t_{max}) = kN_{sub} \tag{9}$$

and therefore

$$t_{max} = Z_j - Z_c \sqrt{\ln\left(N_0 / (kN_{sub})\right)} \tag{10}$$

where $(k \le N_0 / N_{sub})$. It has been our experience that reducing *k* below 5 does not impact the model accuracy and, in some cases, setting *k* as large as 10 or 20 is adequate. We have chosen the conservative value (i.e., $k = 5$) for the results presented later in this paper. From *k*, we compute t_{max} and determine the number of shallow nodeplanes based on Z_j.

To discretize the substrate from the well bottom to the wafer backside (or the epi-bulk interface), *m* "deep" nodeplanes are used. The doping is uniform in this region. The plane-to-plane mesh spacing can be made coarser here because the deep substrate currents generally flow laterally and over distances much greater than typical site-to-site spacings in the (*x*,*y*) nodeplanes. Using 4 nodeplanes in this

region is sufficient. A finer z-discretization for $z > Z_j$ yields identical results in every case we've studied.

D. Model Verification

The new model formulation has been verified by comparing electrical-level simulation results to those obtained using a device simulator called MEDICI [11]. Two device cross-sections were considered. Fig. 4a shows an analog transistor separated from a "noisy node", which represents a MOSFET drain in a digital section. A voltage pulse ($t_r = t_f = 1$ ns) is applied to the noisy node electrode, and switching current is injected across the drain junction directly into the common substrate. A $p+$ ohmic contact collects the noise current which first flows beneath the analog transistor, creating fluctuations in the local substrate potential, V_{sub}. The cross-section shown in Fig. 4b is similar, except that the noisy node is placed inside a diffused n-well. In this case, injected current generated at the noisy node must flow across the well boundary before upsetting the sensitive device.

For circuit simulations, lumped element substrate models were formulated using Voronoi tessellation. Fig. 5 compares the voltage waveforms observed at the substrate node of the sensitive transistor in the two simulations. The macromodeling scheme predicts the transient behavior of V_{sub} accurately.

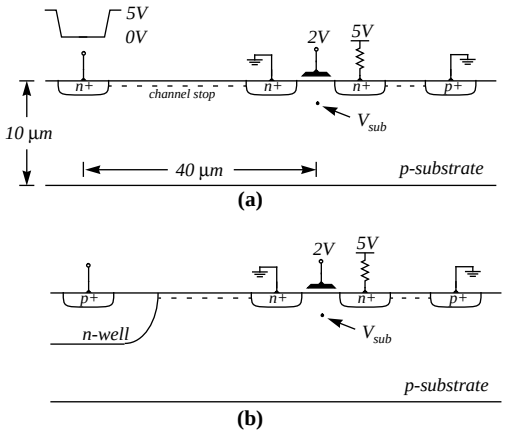


Fig. 4 Cross-sections for model verification via 2-D device simulation. **(a)** A noisy diffusion adjacent to a sensitive analog transistor. **(b)** The same cross-section, except the noisy node is positioned inside a diffused n-well. The substrate doping parameters are: N_{sub}=1.0x10^{15} cm^{-3}, channel stop N_0=3.0x10^{16} cm^{-3} with Z_j=0.20 µm, and n-well N_0=5.0x10^{16} cm^{-3} with Z_j=3.0 µm.

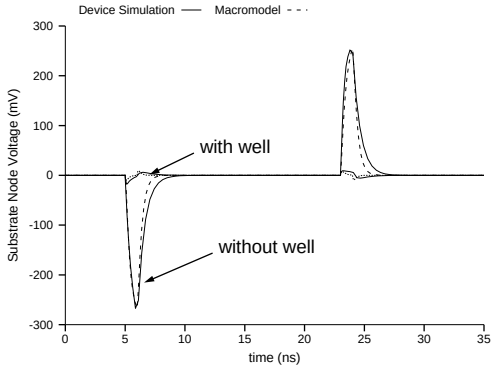


Fig. 5 Results of device simulation and circuit-level simulation using the new substrate macromodel for the cross-sections of Fig. 4.

III. Layout Extraction

Generation of the substrate macromodel is inextricably linked to the circuit layout geometry. Model formulation requires a simulation netlist (i.e., a SPICE input file), a GDSII file containing full-circuit layout data, and a technology file which contains extraction and mesh generation directives. The process outputs a SPICE-compatible subcircuit definition, and modifies the original input netlist to facilitate integration of the circuit and model for post-layout analysis.

The extraction algorithms we use are *edge-based* [12]. A translator first converts the hierarchical GDSII geometric data to files containing the non-overlapping polygon edges for each mask layer. These files contain edge attributes for the so-called *primary* layers. *Scanline* algorithms are used to generate polygons representing *derived* layers, which are boolean combinations of polygons from the primary or previously-derived layers. A scanline algorithm is also employed to identify devices, determine network connectivity, and generate a flattened SPICE-like circuit netlist.

SPICE simulations typically exercise a convention which ties the MOSFET substrate terminals directly to power supply nodes. In noise simulations, circuit operation is obviously sensitive to local substrate voltage variations, so transistor body contacts are attached to external ports of the substrate macromodel. For this purpose, the extracted netlist includes a unique name for the substrate node of each extracted MOSFET. This ensures that each device will be connected to the substrate model at a unique location. Since the user supplies a simulation netlist, the extracted netlist provides a basis for performing topological *A/B* netlist comparison. Network graph isomorphism is used to determine nodename-mapping between the two netlists (for MOSFETs, only the drain, gate, and source nodes are compared). Then, in a flattened version of the original netlist, every transistor substrate nodename is replaced with its extracted equivalent. A similar strategy is employed to handle power supply nodes which contact the model at the substrate and well tie-downs.

The extractor also generates several auxiliary files. These contain polygon edge data for the derived or primary layers representing MOSFET channel regions (with corresponding substrate terminal nodenames), ohmic contacts and guard bands (with corresponding power supply nodenames), and wells. They are used to determine the layout-dependent Voronoi site representation for the chip surface (x,y) nodeplane as discussed in Sections II and IV.

IV. Mixed-Signal Circuit Examples

In this section, the new modeling technique is applied to two mixed-signal circuit examples. In both cases, Voronoi tessellation is used to derive the substrate macromodels directly from GDSII layout data. First, a CMOS ring oscillator is employed to perturb the substrate potential beneath a nearby analog transistor. The design is compact enough to permit a visual representation of the layout and corresponding Voronoi diagram. In the second example, a more complex mixed-signal cell pair is used to demonstrate the *impact* of switching noise on a sensitive analog subcircuit. Both designs are too complex for detailed device simulation, but since the box integration uniform grid macromodel has been independently validated in previous work, we use it to verify the accuracy of the proposed modeling strategy.

A. Ring Oscillator and Analog MOSFET

Fig. 6a shows the layout of a 3-stage ring oscillator and a nearby "sensitive" transistor, based on MOSIS 2.0-µm n-well, double metal scalable CMOS design rules. The layout extractor produces edgefiles for MOSFET channel regions, ohmic contacts, and wells based on suitable extraction directives in a supplied technology file. MOSFET and contact polygon features are used to generate site representations

corresponding to the transistor body terminals and well/substrate ties. Uniformly-spaced sites (Δ = BBOX_SITE_SPACE) are positioned around the layout bounding box. The well edgefiles are used to generate uniformly-spaced straddle sites (Δ = WELL_SITE_SPACE) around the well boundaries and at all well corners.

For more complicated designs, fill sites are used to "seed" the tessellation in areas of the layout where the site density is known to be sparse. Seeding is utilized primarily in routing channels, or in I/O regions which contain little or no active circuitry. In these regions, the substrate electric fields are generally uniform over larger areas, so the density of fill sites can be coarser than in regions characterized by heavy switching activity. Fill site seeding is carried out as follows. First, a uniform (x,y) grid is defined (Δ = FILL_SITE_SPACE). Following the initial site generation, if no layout-derived sites lie closer than FILL_SITE_SPACE to a site on the uniform grid, then that site is inserted into the list of Voronoi sites. BBOX_SITE_SPACE, WELL_SITE_SPACE, and FILL_SITE_SPACE are user-selectable. For this example, BBOX_SITE_SPACE = 15 μm, WELL_SITE_SPACE = 10 μm, and FILL_SITE_SPACE = 50 μm. This particular layout is dense enough to preclude the use of fill sites.

The Voronoi tessellation for the top (*x,y*) nodeplane is shown in Fig. 6b. The same configuration is duplicated for lower nodeplanes. The substrate is 100 μm thick. Delaunay triangulation is used to interconnect adjacent (*x,y*) nodes with branch circuit elements as outlined in Section II. Perpendicular site-to-site elements are added between nodes in adjacent planes. In this example, four shallow and four deep nodeplanes are used. The relevant substrate doping parameters are: N_{sub} = 9.0x10^{14} cm^{-3}, well N_0 = 4.5x10^{16} cm^{-3} with Z_j = 3.5 μm, and channel stop N_0 = 8.0x10^{17} cm^{-3} with Z_j = 0.2 μm.

For simulation, SPICE Level 3 MOSFET models based on parametric test results were obtained from MOSIS. Substrate macromodels were formulated using both a uniform grid (based on box integration), and the model derived via Voronoi tessellation (i.e., that shown in Fig. 6b). The same *z*-discretization was used in both cases. The uniform grid utilized an (*x,y*) site-spacing of 3.0 μm. If a coarser mesh was employed, layout features in some regions were too crowded for the resolution of the grid. The resultant substrate macromodel contains 11,255 nodes. In contrast, the Voronoi tessellation produced a substrate mesh containing only 767 circuit nodes. Additional properties of the generated models appear in Table 1.

The ring oscillator was free-running, and the analog transistor was biased to deliver a constant current in the absence of substrate noise. For noise simulation, we monitored the substrate node of the sensitive device. Fig. 7a shows the voltage waveforms at each inverter output in the ring oscillator. Fig. 7b compares the signals at the substrate terminal of the sensitive transistor which were obtained from the two models. The two approaches yield results which differ by less than 5%. Note that the peaks in the noise waveforms occur when the ring oscillator outputs are changing most rapidly. Also, the maximum noise voltage level is associated with the switching of the oscillator stage closest to the sensitive device.

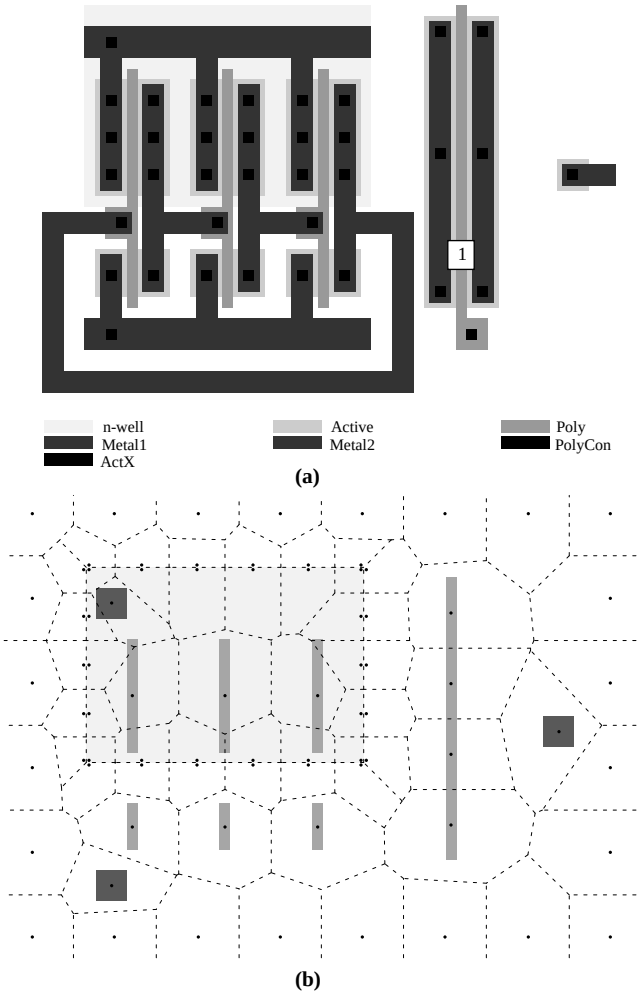


Fig. 6 (a) Layout of a 3-stage ring oscillator and adjacent sensitive "analog" transistor (1). **(b)** The layout-derived Voronoi tessellation.

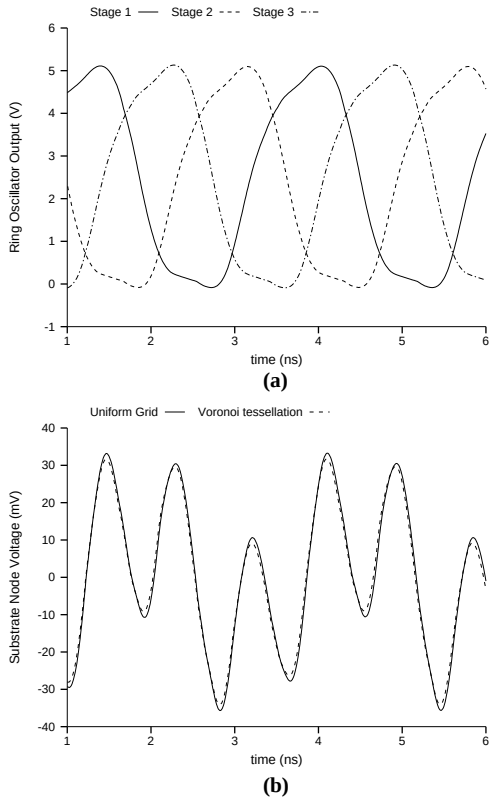


Fig. 7 (a) Simulated voltage waveforms for each stage of the ring oscillator in Fig. 6. "Stage 3" is the inverter closest to the sensitive device. **(b)** Simulated voltage waveforms at the substrate node of the sensitive transistor.

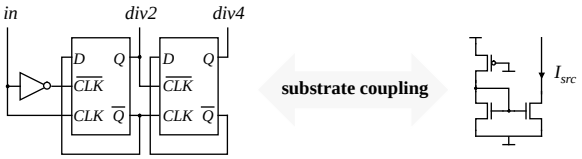
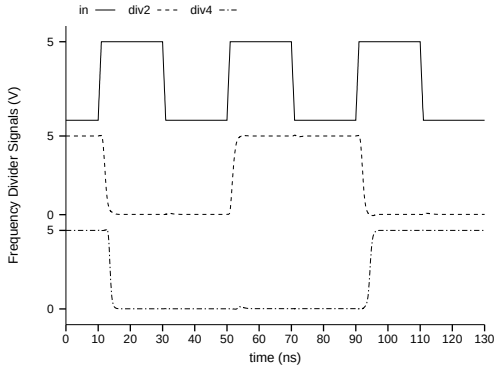
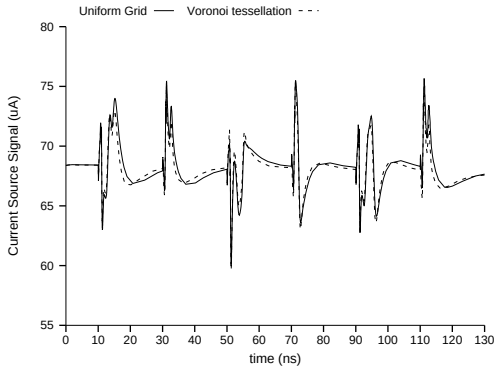


Fig. 8 Digital frequency divider and adjacent analog current source.



(a)



(b)

Fig. 9 (a) Switching waveforms for the frequency divider in Figure 8. **(b)** Simulated current waveforms, I_{src}, for the nearby analog current source.

B. Frequency Divider and Analog Current Source

To assess the impact of noise coupling, it is necessary to monitor the effects of substrate voltage variations on the *performance* of sensitive circuitry. Fig. 8 shows the schematic of a CMOS frequency divider and analog current source which represent nearby cells on a mixed-signal chip. The physical separation is approximately 150 µm. The current source sinks, by design, 68 µA. The circuit was designed using transmission gate flip-flops, analog MOSFETs, and the MOSIS design rules and process parameters described earlier. Macromodels for circuit simulation were extracted from the layout specification, and SPICE was used to obtain voltage waveforms for the divider outputs and to monitor their impact on the current source signal.

The divider circuitry injects substrate current primarily during state transitions (Fig. 9a). The noise is particularly severe because the source signal, which remains constant in the absence of substrate-coupling, deviates from its DC value by more than 20%. The current source waveform, I_{src}, is shown in Fig. 9b, where again, simulation results were obtained for both uniform (3.0 µm) and Voronoi-derived grids. The two modeling approaches yield consistent results.

Table 1 summarizes the macromodel characteristics derived for the two circuit simulation examples presented in this section. Using the new strategy, the model complexity is reduced significantly as compared to rectangular gridding methods previously described. It should be re-emphasized that mesh reduction for large circuit models is *required* as a network pre-conditioner for SPICE simulation. The node count obtained for each model formulation is an important figure-of-merit in light of the CPU and memory requirements imposed by those algorithms. It is also worth noting that the example layouts we present contain no channels for interconnect routing. For larger circuits, the routing region inefficiencies associated with rectangular mesh generation techniques will impact the node count ratio even more.

Table 1: Summary of Model Statistics - Uniform vs. Voronoi Grid

	Uniform (3-µm) Grid			Voronoi-Tessellated Grid			Node Count Ratio
Circuit	Nodes	Resistors	Caps	Nodes	Resistors	Caps	
Osc / MOSFET	11255	31516	544	767	2408	132	0.068
Freq Div / Isrc	55818	157532	3259	3308	10838	641	0.059

V. Conclusion

In this work, we present a novel modeling strategy for incorporating substrate coupling effects into post-layout, mixed-A/D circuit analysis. Substrate models are realized directly from the layout specification using Voronoi tessellation. The derived SPICE-compatible subcircuit networks contain nearly two orders of magnitude fewer circuit nodes than existing models, while retaining the accuracy required for subsequent design verification. This is significant due to the superlinear speed and memory dependence of intermediate network reduction algorithms on the quantity of circuit nodes in the lumped element model. The accuracy has been verified by comparing simulation results to those derived from previously validated models as well as those obtained from device-level simulation. By adopting a universal format for input layout data, and integrating the model generator with a flexible layout extractor, the new methodology provides a practical approach to analyzing substrate-coupled switching noise in mixed-signal circuits.

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