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General Chair's Message

On behalf of the Steering Committee for ACV'95, I would like to welcome you to the joint conference ASP-DAC'95/CHDL'95/VLSI'95.

ASP-DAC'95 is the first in a series of biennial international conferences on Design Automation which have been organized by leading engineers in this field representing Asian and South Pacific countries. In launching the new conference series, the initiators were encouraged and supported by their colleagues in the Design Automation community in not only Asian but also North-American and European countries. Although the ASP-DAC is considered as a sister conference of the DAC (in US) and the EuroDAC, its technical program puts more emphasis on a specific range of design tasks closely related to fabrication and manufacturing in light of the distinctive nature of DA/CAD activities in the Asian and South Pacific region. Topics includes Physical Design, Test Design, Synthesis, Manufacturing, Design Environment, User-Oriented Issues, etc.

Both CHDL and VLSI are biennial conference series sponsored by the IFIP TC10 Working Group 10.5 started in 1973 and 1975, respectively. The emphasis of CHDL is placed on Formal Methods, Verification, Hardware Description Languages, and the Methodology surrounding their use. The VLSI is aiming at the exchanging new ideas lying between System Architecture, Design Methods, and VLSI Technologies to make long stride up to the new century. It is our great pleasure that both of the IFIP conferences return to Japan after they were held in Tokyo in 1985.

A total of 201 papers from 29 countries have been submitted to the joint conference and a total of 117 of them have been accepted for presentation at the ASP-DAC, CHDL or VLSI. The Technical Program Committee was formed for each conference chaired by Professors I. Shirakawa (ASP-DAC), S. Johnson (CHDL), and W. Rosenstiel (VLSI). They have assigned three tracks for ASP-DAC, one track for CHDL, and another for VLSI, and the technical program layout is arranged so as to minimize possible topical conflict among sessions. In addition to the contributed papers, each conference features special sessions and invited talks on up-to-date topics. The time-consuming and tough effort of the program committee members under the leadership of the three Program Chairs yields the quality technical programs.

To offer some timely technical topics with an insight into current and future business environment, the first session of each day features an attractive keynote speaker; Dr. A. Asada (Sharp) on August 30, Dr. J. Meadlock (Intergraph) on August 31, and Dr. J. Darringer (IBM) on September 1. The joint conference also offers five tutorials running in parallel on August 29 to introduce the attendees and novice engineers to basic concepts, relevant issues and some possible solutions in their topical areas.

EDA Techno Fair'95 (the third of the annual premier Japanese EDA show) is collocated with the ACV'95. Exhibitors included are companies involved in the sales of EDA tools/systems as well as related products or services. A unique feature of the exhibition is the University Plaza, where more than ten Japanese Universities demonstrate their education/ research products. The exhibition is sponsored by the Electronic Industries Association of Japan (EIAJ) and organized by volunteering effort of engineers in leading electronic industries in Japan under the leadership of Dr. K. Yoshida.

The venue of the joint conference and the exhibition is the Nippon Convention Center in Makuhari Messe, which is located at a convenient place to access by train or car within 30 minutes from either Tokyo station or Narita Airport.

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ASP-DAC'95 Program Chair's Message

On behalf of the TPC (Technical Program Committee), I would like to invite you to ASP-DAC'95, which is the first in a series of biennial international conferences on design automation to be held in Asia and South Pacific Area. Thanks to great efforts of TPC Members distributed all over the world, the response to our Call-For-Papers was 107 submissions from 20 countries, of which we were able to accept almost 60% for regular and short papers. The Technical Program is structured under three parallel tracks; two for Regular Tracks and one for Special Track. Most of accepted papers are included in the Regular Tracks, and special sessions and panel sessions are incorporated into the Special Track whenever the topics are appropriate. The TPC believes that the highest technical standard of the submitted papers reflects the importance of this Conference and its location in the fastest developing area of the high-technology world.

Finally, the TPC would like to thank the authors for their excellent works that ultimately make ASP-DAC a premier conference to present the latest advances in the field of design automation.

Isao Shirakawa
Program Chair, ASP-DAC'95

Best Paper Award Candidates
Asia and South Pacific Design Automation Conference 1995 (ASP-DAC '95)

Category-1: Physical-Level Design Automation

2B.1 A Framework for the Analysis and Design of Algorithms for a Class of VLSI-CAD Optimization Problems
C. J. Shi, J. A. Brzozowski (Univ. of Waterloo, Canada)

4A.1 Region Definition and Ordering Assignment with the Minimization of the Number of Switchboxes
Jin-Tai Yan (National Chiao Tung Univ., Taiwan)

5A.1 Extending Pitchmatching Algorithms to Layouts with Multiple Grid Constraints
Hiroshi Miyashita (NTT, Japan)

6A.2 Maple-opt: A Simultaneous Technology Mapping, Placement, and Global Routing Algorithm for FPGAs with Performance Optimization
Nozomu Togawa, Masao Sato, Tatsuo Ohtsuki (Waseda Univ., Japan)

7A.3 A Model-Adaptable MOSFET Parameter Extraction System
Masaki Kondo, Hidetoshi Onodera, Keikichi Tamaru (Kyoto Univ., Japan)

8A.2 New Performance Driven Placement Method with the Elmore Delay Model for Row Based VLSIs
Tetsushi Koide, Mitsuhiro Ono, Shinichi Wakabayashi, Yutaka Nishimaru (Hiroshima Univ., Japan), Noriyoshi Yoshida (Hiroshima City Univ., Japan)

8A.4 Fanout-Tree Restructuring Algorithm for Post-Placement Timing Optimization
T. Aoki, M. Murakata, T. Mituhashi, N. Goto (Toshiba Corp., Japan)

Category-2: Logic-Level Design Automation

2B.3 A Hardware/Software Codesign Method for Pipelined Instruction Set Processor Using Adaptive Database
Nguyen Ngoc Binh, Masaharu Imai, Akichika Shiomi (Toyohashi Univ. of Technology, Japan), Nobuyuki Hikichi (Software Research Associates, Inc., Japan)

3B.1 Power Analysis of a 32-bit Embedded Microcontroller
Vivek Tiwari (Princeton Univ., USA), Mike Tien-Chien Lee (Fujitsu Labs. of America, USA)

4B.1 Design for Testability Using Register-Transfer Level Partial Scan Selection
Akira Motohara, Sadami Takeoka, Toshinori Hosokawa, Mitsuyasu Ohta, Yuji Takai, Michihiro Matsumoto, Michiaki Muraoka (Matsushita Electric Industrial Co., Ltd., Japan)

4C.2 Logic Optimization by an Improved Sequential Redundancy Addition and Removal Technique
Uwe Glaser (Schloss Birlinghoven, Germany), Kwang-Ting Cheng (Univ. of California, Santa Barbara, USA)

5B.4 Logic Rectification and Synthesis for Engineering Change
Chih-Chang Lin, David Ihsin Cheng, Malgorzata Marek-Sadowska (Univ. of California, Santa Barbara, USA), Kuang-Chien Chen (Fujitsu Labs. of America, Inc., USA)

6B.2 GRMIN: A Heuristic Simplification Algorithm for Generalized Reed-Muller Expressions
Debatosh Debnath, Tsutomu Sasao (Kyushu Inst. of Technology, Japan)

9B.3 Synthesis-for-Testability Using Transformations
Miodrag Potkonjak, Sujit Dey, Rabindra K. Roy (NEC USA, USA)

Keynote Address I

Business Strategies for the Era of Multimedia

Atsushi Asada
Senior Executive Vice President, Sharp

Multimedia technology and infrastructure are furthering each other's rapid development, and an immense multimedia market is beginning to emerge.

In this multimedia era, our company is pursuing "Multimedia for the individuals" and trying to provide next generation multimedia systems by developing both key technologies and products, particularly those targeted for personal use.

In this presentation, we show current trends in multimedia technologies and our strategies for this market.

Keynote Address II

The EDA Design Environment of the Future

Jim Meadlock
CEO, Intergraph

Windows and Windows NT will provide an environment for EDA engineering which will bring cost-effective design capability to each step in the design and manufacturing process. This environment will also permit the integration and network support of standard office products with the design process. We will present the status and future direction of our efforts toward providing tools which offer this new capability.

Keynote Address III

Designing Million Gate ASICs

John Darringer
Director, EDA, IBM

Million gate ASICs are being designed, manufactured, and used to achieve new levels of system integration and performance. Drawing on real design experiences, we will discuss the challenges of this task including planning the chip layout, achieving the desired performance, and testing these chips in manufacturing. This demanding high-end ASIC market is the proving ground for tomorrow's EDA tools.

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Seung-Ho Hwang
KAIST, Korea

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Takeshi Onodera
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This event has been organized with the aggressive intention of combining the newly founded conference (ASP-DAC) and the traditional conferences (CHDL and VLSI) with the industry exhibition (EDA Technofair) all at the Makuhari Messe. The joint conference is co-sponsored by several academic entities in Japan, US and Europe, and the exhibition is conducted by the EIAJ. In preparing the ASP-DAC'95/CHDL'95/VLSI'95 with EDA Technofair'95, we have been heavily relied upon the continuing, collaborative effort of many people representing various organizations all over the world. I would like to take this opportunity to thank Messrs. T. Kozawa and S. Murai and all the Steering Committee, Organizing Committee and Technical Program Committee members for their volunteering service.

I hope you enjoy not only the joint conference but also the various events organized in conjunction with it.

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