Design Automation for Integrated Continuous-Time Filters using Integrators

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Abstract— This paper proposes a design automation for filters using integrators. This is based on a predistortion without knowledge of a filter topology. The predistortion requires an integrator having the same structure, the same-value elements and an electrically controllable unity-gain frequency, and compensates for the deviation of frequency characteristics due to an excess phase shift of an integrator. The effectiveness of the proposed method is demonstrated through SPICE simulations. An algorithm for a filter design automation is also discussed.

I. Introduction

A design automation for analog circuits is strongly desired to compensate for the shortage of analog circuit designers. The development of such a tool is delayed by complicated specifications for analog circuits and too many choices of circuit structures, etc. To solve these problems many attempts have been made [1]. While analog circuit designs are complicated in general, a filter design is relatively easy, because its specifications are simpler and its synthesis theory has almost been completed. Some methods to integrate filters on a monolithic chip have also been proposed [2], [3]. Nevertheless, there does not exist a filter design considering a layout, compaction, routing, etc., which are peculiar to integrated circuits.

This paper proposes a filter design using integrators, considering the deviation due to an excess phase shift of an integrator. The proposed method employs an integrator having the same structure, the same-value elements and an electrically controllable unity-gain frequency. Furthermore, as an outstanding feature, the method requires no information of a filter topology. In other words, the method can predistort frequency characteristics in advance of determining a filter topology. These facts will relax problems relating to compaction, routing, etc., because the layout problem of a filter can be replaced by that of an integrator.

First, it is proved that an effect due to an excess phase shift of an integrator, for example, caused by a finite gain-bandwidth product of an operational amplifier, becomes equivalent to the replacement of complex variable s to a function $F(s)$ under some conditions in spite of a filter topology. Second, an integrator using MOS Resistive Circuit (MRC) [4] is confirmed to satisfy the conditions. Third, a predistortion based on the mapping of s to $F(s)$ is proposed and simulation results are shown to demonstrate the effectiveness of the proposed method. Last, an algorithm for a filter design automation is discussed.

II. Effect due to Excess Phase Shifts of Integrators

An integrator used here as an example is shown in Fig. 1 where the superscript "i" is added to the parameters related to the i-th integrator in an n-th order filter. Assume that an operational amplifier is ideal, the output voltage $v_{out}^{(i)}$ becomes

$$v_{out}^{(i)} = -\frac{G_1^{(i)} - G_2^{(i)}}{sC^{(i)}} \left(v_{in1}^{(i)} - v_{in2}^{(i)} \right). \tag{1}$$

Since an unity-gain frequency depends on both $G_1^{(i)} - G_2^{(i)}$ and $C^{(i)}$, the frequency can be adjusted by controlling only $G_1^{(i)} - G_2^{(i)}$ under the condition

$$C^{(i)} = C \tag{2}$$

for $i = 1$ to n.

A practical operational amplifier has finite input impedance, nonzero output impedance, finite gain-bandwidth product (GB product), etc. Among these non-idealities, a GB product generally has the most drastic effect on frequency characteristics. Therefore, only a finite GB product is hereafter taken into account and the other parameters are assumed to be ideal. Under this assumption, Eq. (1) can be rewritten in the form

$$v_{out}^{(i)} = -\frac{G_1^{(i)} - G_2^{(i)}}{F^{(i)}(s)C} \left(v_{in1}^{(i)} - v_{in2}^{(i)} \right) \tag{3}$$

where

$$F^{(i)}(s) = s + \frac{1}{Ad(s)}\left(\frac{G_1^{(i)} + G_2^{(i)}}{C} + s\right) \tag{4}$$

and $Ad(s)$ is the gain of the operational amplifier.

It is reasonable to assume that all operational amplifiers used in a filter have the same gain $Ad(s)$ especially on integrated circuits. Furthermore, if the sum of the conductances $G_1^{(i)}$ and $G_2^{(i)}$ is constant, that is

$$G_1^{(i)} + G_2^{(i)} = G_{total} \ , \tag{5}$$

then $F^{(i)}(s)$ becomes

$$F^{(i)}(s) = s + \frac{1}{Ad(s)}\left(\frac{G_{total}}{C} + s\right). \tag{6}$$

Therefore, every $F^{(i)}(s)$ for each integrator becomes the same function $F(s)$ defined by

$$F(s) \stackrel{\text{def}}{=} F^{(i)}(s). \tag{7}$$

From the comparison of Eq. (1) and Eq. (3), it should be noted that the effect of a GB product of an operational amplifier is equivalent to the replacement of the complex variable s by $F(s)$. Thus the transfer function of a filter using nonideal integrators, the characteristics of which is given by Eq. (3) and Eq. (6), is easily calculated by

$$T_{GB}(s) = T(F(s)) \tag{8}$$

where $T(s)$ is the transfer function of the same filter when all integrators are assumed to be ideal. No knowledge about a filter topology is required to obtain Eq. (8) and the effect of a finite GB product can be estimated before determining a filter topology.

In order to realize an integrator with electrically controllable unity-gain frequency, the use of an MRC (Fig. 2) is quite effective. An MRC can be employed for the substitution of four resistors in Fig. 1. It is well known that an MRC has high linearity under $V_3 = V_4$ in Fig. 2 and the equivalent transconductance can be controlled by $V_{G1} - V_{G2}$. An integrator using an MRC is shown in Fig. 3.

For the analysis of the integrator, the linear equivalent circuit of a MOSFET in Fig. 4 [5], which includes parasitic capacitors, is introduced. C_t is the total capacitance between the gate and substrate and $R_{tj}^{(i)}$ is channel resistance given by

$$R_{tj}^{(i)} = \frac{1}{2K(V_{Gj}^{(i)} - V_{th})} \tag{9}$$

where $V_{Gj}^{(i)}$ is the gate voltage and K and V_{th} are MOSFET parameters usually used. From Fig. 4, the function $F^{(i)}(s)$ of the i-th integrator using an MRC is calculated as

$$F^{(i)}(s) = s + \frac{1}{Ad(s)}\left\{\frac{2KV_{total}}{C} + s\left(1 + \frac{C_{total}}{C}\right)\right\} \tag{10}$$

where

$$V_{total} = V_{G1}^{(i)} + V_{G2}^{(i)} - 2V_{th} \tag{11}$$

$$C_{total} = \frac{2}{3}C_t. \tag{12}$$

C_{total} is thought to be constant for each integrator if MOSFETs in MRCs have the same size. Furthermore, if the voltage V_{total} is constant, $F^{(i)}(s)$ becomes the same function for all integrators. Even though this condition is satisfied, unity-gain frequencies are electrically controllable by suitable selection of $V_{G1}^{(i)} - V_{G2}^{(i)}$. These control voltages $V_{G1}^{(i)}$ and $V_{G2}^{(i)}$ can be easily obtained by the common-mode feedback circuit shown in Fig. 3 of [6] with a series of resistors between output terminals as shown in Fig. 5. This makes $(V_{G1}^{(i)} + V_{G2}^{(i)})/2$ equal to a constant reference voltage and $V_{G1}^{(i)} - V_{G2}^{(i)}$ is determined by the resistance ratio.

Thus, frequency characteristics of the filter using only the integrators shown in Fig. 3 can be easily evaluated in advance of determining a filter topology, being considered the effect of finite GB product. Furthermore, it should be noted that the layout problem of such a filter leads to that of an MRC-based integrator because the integrator has the same structure and the same-value elements regardless of its unity-gain frequency.

III. An Example of Predistortion

A. Predistortion of Poles and Zeros

Consideration about poles and zeros is important for predistortion of frequency characteristics.

Let j-th pole ($1 \le j \le n$) and k-th zero ($1 \le k \le m$) of $T(s)$ be p_j and z_k respectively. According to these definitions, $T(s)$ can be written in the form

$$T(s) = H\frac{\prod_{k=1}^{m}(s - z_k)}{\prod_{j=1}^{n}(s - p_j)} \tag{13}$$

and $T_{GB}(s)$ becomes

$$T_{GB}(s) = H\frac{\prod_{k=1}^{m}(F(s) - z_k)}{\prod_{j=1}^{n}(F(s) - p_j)}. \tag{14}$$

Generally $F(s)$ is a rational function expressed by

$$F(s) = \frac{N_F(s)}{D_F(s)} \tag{15}$$

where $N_F(s)$ and $D_F(s)$ are polynomials. Substitution of Eq. (15) gives

$$T_{GB}(s) = H \frac{(D_F(s))^{n-m} \prod_{k=1}^{m} (N_F(s) - z_k D_F(s))}{\prod_{j=1}^{n} (N_F(s) - p_j D_F(s))}. \quad (16)$$

Consequently the poles and zeros of T_{GB} are respectively given as the solutions of

$$N_F(s) - p_j D_F(s) = 0 \quad (1 \le j \le n), \quad (17)$$

$$N_F(s) - z_k D_F(s) = 0 \quad (1 \le k \le m), \quad (18)$$

and

$$D_F(s) = 0. \quad (19)$$

From these equations it is clear that the number of poles or zeros in $T_{GB}(s)$ is lager than in $T(s)$. Among these poles and zeros, n poles and m zeros should be placed at ideal positions on s plane. This placement will predistort frequency characteristics because the other poles and zeros are far from ideal poles and zeros and affect the frequency characteristics of $T_{GB}(s)$ little. In order to place n poles and m zeros at ideal positions, the denominator for ideal poles and the numerator for ideal zeros must be 0. That is, from Eq. (16),

$$\prod_{j=1}^{n} (N_F(z_{ideal,i}) - p_j D_F(z_{ideal,i})) = 0 \quad (20)$$

$$(D_F(z_{ideal,k}))^{n-m} \prod_{k=1}^{m} (N_F(z_{ideal,i}) - z_k D_F(z_{ideal,i})) = 0 \quad (21)$$

must be satisfied for all i where $p_{ideal,i}$ are i-th ideal pole and $z_{ideal,i}$ i-th ideal zero. By solving these equations, poles and zeros of $T(s)$ can be obtained as

$$p_i = \frac{N_F(p_{ideal,i})}{D_F(p_{ideal,i})} = F(p_{ideal,i}) \quad (22)$$

and

$$z_i = \frac{N_F(z_{ideal,i})}{D_F(z_{ideal,i})} = F(z_{ideal,i}). \quad (23)$$

Consequently, if the transfer function $T(s)$ is designed by the poles and zeros given by Eq. (22) and Eq. (23), the transfer function $T_{GB}(s)$ will be predistorted so as to have ideal poles and zeros suitable for specifications.

B. Simulation Results

A 5-th order leapfrog low-pass filter with 0.5-dB passband ripple and 20-kHz cutoff frequency is simulated. The ideal poles $p_{ideal,j}$ $(j = 1, 2, \cdots, 5)$ are placed on the ellipse.

Assume that the gain $Ad(s)$ of an operational amplifier is expressed by

$$Ad(s) = \frac{2\pi GB}{s + \omega_c} \quad (24)$$

where $\omega_c/(2\pi)$ and GB are a cutoff frequency and a GB product of an operational amplifier, respectively. From this assumption, $F(s)$ becomes

$$F(s) = s + \frac{(s + \omega_c)(\alpha s + \beta)}{2\pi GB} \quad (25)$$

where

$$\alpha = 1 + \frac{C_{total}}{C} \quad (26)$$

$$\beta = \frac{2KV_{total}}{C}. \quad (27)$$

For the predistortion, the poles p_j of $T(s)$ is set to be

$$p_j = F(p_{ideal,j}) \quad (28)$$

for $j = 1, 2, \cdots, 5$.

In this case, the other parasitic poles $p_{para,j}$ of $T_{GB}(s)$ can be obtained by solving

$$F(s) - F(p_{ideal,j}) = 0 \quad (29)$$

as

$$p_{para,j} = -\frac{2\pi GB + \alpha\omega_c + \beta}{\alpha} - p_{ideal,j} \quad (30)$$

for $j = 1, 2, \cdots, 5$. As is seen from the above equation, the parasitic poles are thought to be located far from the ideal ones if GB is relatively large.

The capacitance C is selected to be 1pF and every length and width of MOSFETs in all MRCs, except ones for a 3-input integrator, are 100μm and 5μm, respectively. In case of the 3-input integrator, the width of MOSFETs is 2.5μm since the integrator requires two MRCs.

The simulation result in case of GB = 1MHz and 80dB DC gain is illustrated in Fig. 6 together with the ideal and the uncompensated cases. The figure shows the effectiveness of the proposed method. Parasitic poles affect the frequency characteristics at frequencies more than 1MHz.

IV. A Procedure of Design Automation

The proposed method makes filter CAD quite easy, because the method is independent of a filter topology and integrators have the same structure as well as the same-value elements for any specifications.

The flowchart of the proposed design automation using integrators is shown in Fig. 7. At the first design stage, according to the given specifications, an integrator is selected from "integrator library", if some other integrators than Fig. 3 are registered in the library. The library has the data for integrators, such as the function $F(s)$, layout, etc. At the next stage, the transfer function of the filter

can be predistorted according to the function $F(s)$ before a topology of a filter is decided. Since $F(s)$ is identical for any specifications, $F(s)$ can be used repeatedly and refined by the implementation results. The refinement of $F(s)$ results in the improvement of predistortion capability of the proposed method. Finally, a topology of a filter is selected from "filter library" by a circuit designer and a filter is implemented. The layout of the filter is just the connection of each integrator since all integrators have the same layout and this data is stored in "integrator library".

V. Conclusions

This paper has made an attempt for a design automation of integrated continuous-time filters. For this attempt, a predistortion for filters using integrators has been proposed and its effectiveness has also been demonstrated through SPICE simulations. An algorithm for a filter design automation has been presented as well.

The proposed method compensates for the deviation due to an excess phase shift of an integrator without knowledge of a filter topology. In addition to that, the method requires only an integrator having the same structure, the same-value elements and an electrically controllable unity-gain frequency. From these facts, the method is thought to relax the layout problem relating to compaction, routing, etc, which are peculiar to integrated circuits, because the layout of a filter is simply replaced by that of an integrator.

Although this paper has employed an integrator using MRC as an example, the proposed method is applicable to other integrators, for example an integrator based on bipolar process. "Integrator library" will be provided in the near future.

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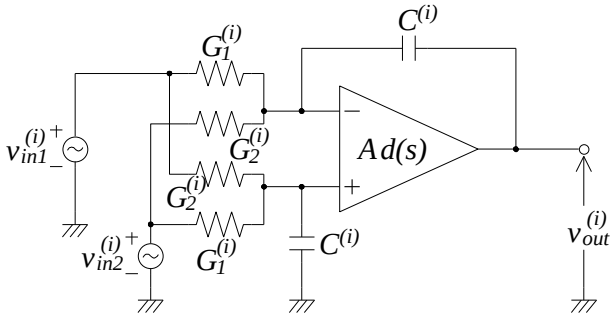

Fig. 1. Example of an integrator

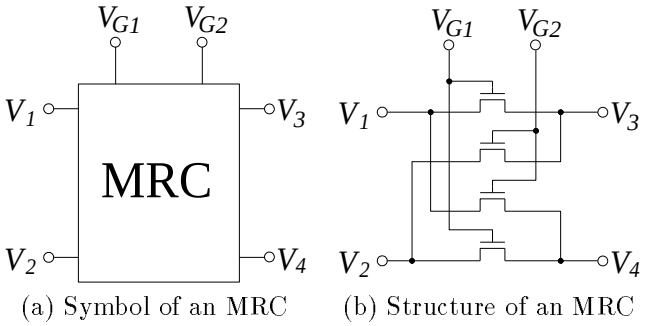

Fig. 2. MRC

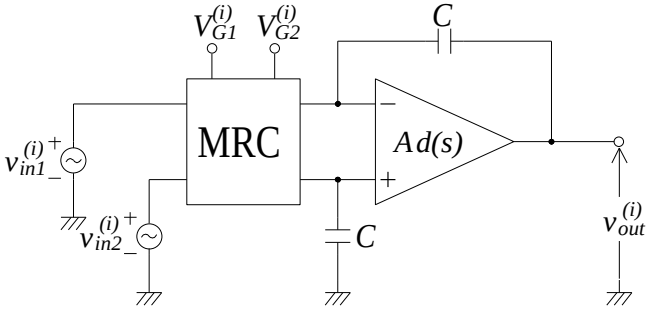

Fig. 3. Integrator with an MRC

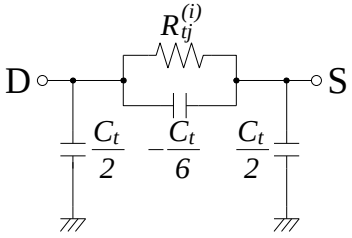

Fig. 4. Linear equivalent circuit of a MOSFET

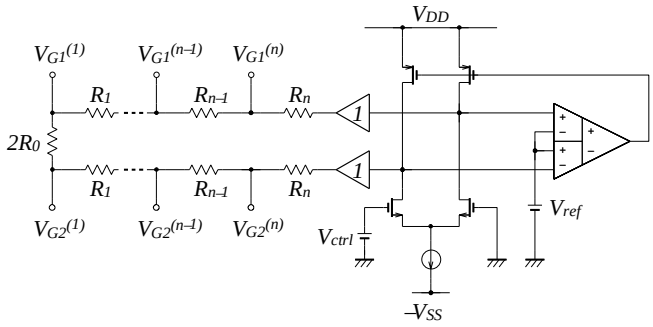

Fig. 5. Controll voltages generator with a DDA

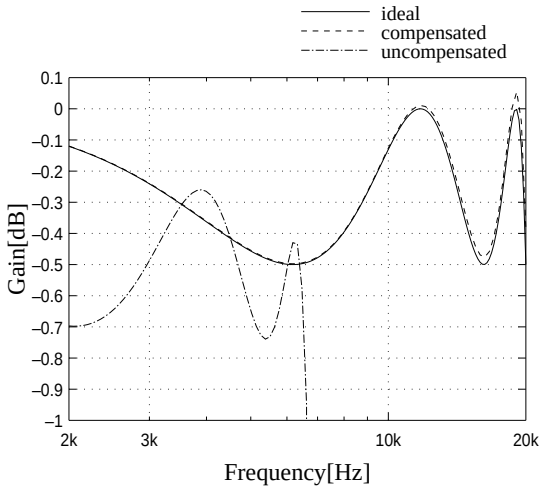

Fig. 6. Simulation results

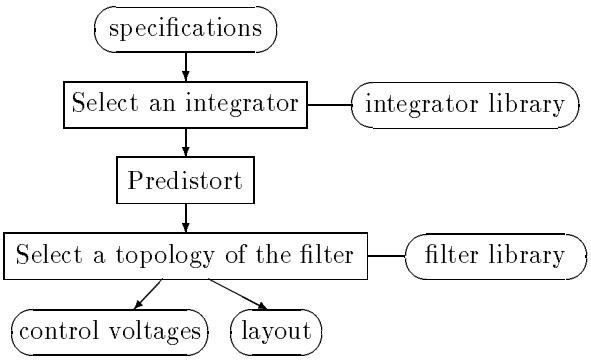

Fig. 7. Flowchart