An Efficient Logic/Circuit Mixed-Mode Simulator for Analysis of Power Supply Voltage Fluctuation

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Abstract--- A **mixed-mode simulator is described that can simulate voltage fluctuations in the power supply network. Current flow due to logic events is taken into account in order to predict the voltage fluctuations. The difference between the maximum voltage fluctuations calculated by the proposed mixed-mode simulation and these calculated by conventional circuit simulation are within 20%, and we demonstrated the feasibility of the proposed simulation by simulating an entire MOS memory chip (36,000 transistors) in 75 minutes on an HP9000/735.**

I. Introduction

The increased scale and complexity of LSI's has made it necessary to analyze VLSI circuits in more detail because of the many second-order effects caused by parasitic elements. Power supply network voltage fluctuations, for example, can become a serious problem by causing noise to propagate through the power supply network and thus cause signal errors. To evaluate this problem before producing the actual chip, it is necessary to simulate the voltage fluctuations of the whole chip.

A method for simulating the voltage fluctuations in a resistive power supply network has already been reported [1]. In this method, the currents that enter the power supply are calculated and applied to the resistor network. Then each node voltage of the network is calculated. This method, however can be used only with power supply networks that consist only of resistors and cannot be used with networks that include capacitors. Another method models the current of cells as a bell-shaped envelope current and the supply current is calculated by using a logic simulator [2]. A problem with both of these methods is that because only the power network is considered when calculating node voltages, the influence of voltage fluctuations on other parts of the designed circuit cannot be simulated.

It is difficult to simulate an entire circuit quickly because using a circuit simulator requires enormous amounts of CPU time and memory. An effective way to do such simulations, though, is to use a mixed-mode simulator. Recently reported glued mixed-mode simulators use a loosely coupled circuit simulator and logic simulator. The circuit simulator is used to precisely analyze the critical path of digital circuits or the analog portion of analog-digital mixed circuits, and the logic simulator is used to roughly analyze the rest of the circuit where precision is less important [3-7].

In this paper we present a new voltage fluctuation analysis method that uses a glued logic/circuit mixed-mode simulator. Since conventional logic simulators cannot take power supplies into consideration, we present a source current model that calculates the current flowing into the power supply network when a logic event simulated by the logic simulator occurs. This current flow is then incorporated into the circuit simulation so that voltage fluctuation can be predicted accurately.

II. Outline of the Mixed-mode Simulator

This mixed-mode simulator consists of five parts. The first four are used in conventional mixed-mode simulation, but the current calculator is new and is used to simulate the source current of the logic gates by applying the source current model.

1) A SPICE-like circuit simulator that simulates the portion of the circuit described at the transistor level.
2) An event-driven logic simulator that simulates the portion of the circuit described at the gate level.
3) A controller of these two loosely coupled simulators. Since the two simulators use different simulation methods, it is necessary to synchronize them so that signals can be transfered between them and so that the simulation can be switched between the two simulators. In this mixed-mode simulator, the lock-step method[4] is use for synchronization.
4) An analog-to-digital and digital-to-analog signal converter. Since the logic simulator can handle only high-level or low-level signals, whereas the circuit simulator can deal with signals of any level, it is necessary to convert signals during mixed-mode simulation.
5) A source current calculator that responds to the occurrence of a logic event generated by the logic simulator and, according to the kind of logic event, calculates the current that flows into the power supply network.

The flow of the mixed-mode simulation is shown in Fig. 1. The basic idea of a glued simulator is to let one simulator run first with the other following it at intervals. In this mixed-mode simulator, the logic simulator goes first, and the circuit simulator follows. Logic events at the DA (Digital-to-Analog) interface and circuit events at the AD (Analog-to-Digital) interface are transferred during simulation.

Consider a mixed-mode simulation using the circuit shown in Fig. 2 and suppose, for instance, that the gate level circuit in Fig. 2(b) is simulated until time Tl1 and an event of gate G1 is generated at time Tl1. Then the event time of gate G1 and the event type (from low to high or from high to low) will be transferred to the signal converter and current calculator. In this case, the signal name S1, event time Tl1, and event type (from high to low) will be transferred. When the circuit simulator runs from time 0 to time Tc1, the input current for the DA interface signal and source current will be incorporated into the circuit simulation (Fig. 2(e)). The generated DA interface signal will be the input to the source current Ida and the source currents for gate G1 will be the inputs to the current sources Ivcc and Ignd. Incorporating the source currents for gate G1 enables this simulator to be used to analyze influence of this fluctuation on other parts of the circuit. The two simulators run alternately until the end of the analysis.

III. Triangular Source Current Model for CMOS Gates

The source current of a CMOS logic gate can be divided into four types according to the event type and source type. When the output of the gate changes from low to high, the current to charge the load capacitance as well as the current flowing through the NMOS transistor will flow through the PMOS transistor. When the output of the gate changes from high to low, the current to discharge the load capacitance as well as the current flowing through the PMOS transistor will flow through the NMOS transistor.

The easiest way to model the source current is to extract the waveform of the source current for each gate and create a look-up table. But for various reasons this is not efficient: If the circuit is large, creating a look-up table for every gate requires a huge amount of memory, and it takes time to extract the source current parameters of all the gates. And when mixed-mode simulation is used in the design environment, the design of the circuit and the subsequent simulations are continually changed. The channel length or width of the MOS transistors, for example, might be changed in each simulation. Changing any of the parameters means re-extracting the source current.

We therefore need a simple source current model that can also be adjusted easily when the size of the transistor or the load capacitance is changed. Because the shape of the source current waveform is quite similar to a triangle, we approximate the source current by using a triangular current model. The parameters for this model are calculated only for basic gates in the circuit being simulated. Parameters for the models of the other gates with the same topology but with different transistor size or load capacitance are based on the model of the basic gates.

When the circuit simulator calculates the triangular source current at a certain simulation time, the following four pieces of information (Fig. 3) are needed:

1) Tstart: The interval between the time that the source current begins flowing (Ts) and the time that the event of the logic gates occurs (Tl).
2) Tpeak: The interval between the time that the event of the logic gates occurs (Tl) and the time that the source current reaches the peak current (Tp).
3) Ipeak: The peak current value of the source current .
4) Tend: The interval between the time that the event of the logic gates occurs (Tl) and the time that the source current stops flowing (Te).

The current that flows through a MOS transistor can be described by the following equations:

$$Id = \frac{\mu\, Cox\, W}{2L}\{2(Vgs - Vt)Vds - Vds^2\} \quad \text{(Linear region)} \qquad (1)$$

$$Id = \frac{\mu\, Cox\, W}{2L}\{2(Vgs - Vt)^2\} \quad \text{(Saturation region)} \qquad (2)$$

where
W is the channel width of the MOS transistor,
L is the channel length of the MOS transistor,
Vgs is the voltage between the gate and source,
Vds is the voltage between the drain and source,
Vt is the threshold voltage,
μ is the mobility, and
Cox is the gate oxide capacitance.

The source current of CMOS gates are thus determined by the following factors:

1) W, the channel width of the MOS transistor.
2) L, the channel length of the MOS transistor.
3) Cld, the load capacitance of the gate.
4) Vcc, the voltage of the power supply.
5) Tr, Tf, the rise and fall times of the input.

The model parameters are initially calculated for typical gates, and the source current for gates that have different W, L, Cld, and Vcc value is adjusted with the methods described in the rest of this section. (In this paper, differences due to variations in the rise and fall times are ignored.)

1) Channel width: As shown in Equations (1) and (2), both in the linear and in the saturation regions, the current that flows into a MOS transistor is proportional to the channel width. As shown in Fig. 4(a), the peak of the source current increases with increasing channel width. When the width of the MOS channel is changed, the peak of the source current is calculated as follows:

$$IWpeak = \frac{W}{W0} Ipeak0, \qquad (3)$$

where
W is the channel width of the MOS transistor to be used in mixed-mode simulation,
W0 is the channel width of the basic MOS transistor for which the model parameters were extracted,
IWpeak is the peak of the source current when the channel width is W, and
Ipeak 0 is the peak of the source current when the channel width is W0.

The total charge stored by the load capacitance is almost constant and can be described as

$$\text{Total charge} = Q = (Vcc\text{-}Vgnd)\,Cld0\,, \quad (4)$$

where

Vcc is the voltage of the power supply,
Vgnd is the voltage of the ground, and
Cld0 is the load capacitance for the basic model from which parameters were extracted.

The total charge can be calculated as the area of the current triangle:

$$Q = \frac{(Tstart + Tend)IWpeak}{2} = (Vcc - Vgnd)Cld0 \quad (5)$$

The time that the current stops flowing (Tend) can be calculated as follows :

$$Tend = \frac{2(Vcc - Vgnd)Cld0}{IWpeak} - Tstart \quad (6)$$

The time when the current starts flowing (Tstart) is not adjusted because, as shown in Fig. 4(a), it does not change with changes in channel width. This figure also shows that the time the current reaches the peak value (Tpeak) need not be adjusted according to the channel width, as long as the difference in Tpeak is negligible when the channel width is changed.

2) Channel length: The source current of the gates when the channel length is changed is adjusted as follows. As shown in Equations (1) and (2), in the linear and saturation regions, the current that flows into a MOS transistor is inversely proportional to the channel length. And as shown in Fig. 4(b), the peak of the source current decreases with decreasing channel length. The peak of the source current when the length of the MOS channel changes is calculated as follows:

$$ILpeak = \frac{L0}{L}Ipeak0, \quad (7)$$

where

L is the channel length of the MOS transistor to be used in mixed-mode simulation,
L0 is the channel length of the basic MOS transistor for which the model parameters were extracted,
ILpeak is the peak of the source current when the channel length is L, and
Ipeak 0 is the peak of the source current when the channel length is L0.

Again, the charge stored by the load capacitance is almost constant, and the time when the current stops flowing (Tend) is calculated using Equation (6) with ILpeak substituted for IWpeak .

The time that the current starts flowing (Tstart) is not adjusted, because it is not affected by changes in channel length. The time that the current reaches the peak value (Tpeak) is also not adjusted for changes in channel length, as justified from Fig. 4(b) showing that the change in Tpeak for different channel lengths is small enough to be ignored.

3) Load capacitance: When the fanout is changed, the equivalent load capacitance will also change and the waveform of the source current will change as shown in Fig. 4(c). The current drive is constant, and only the amount of charge will change as the capacitance changes. So the triangular current when the load capacitance is Cld, can be derived as follows:

$$Tend = \frac{2(Vcc - Vgnd)Cld}{Ipeak0} - Tstart\,, \quad (8)$$

where

Cld is the load capacitance when mixed-mode simulation is processed.

The time that the current starts flowing (Tstart), the time that the current reaches the peak (Tpeak), and the peak current value (Ipeak) are not adjusted because they are not affected by changes in load capacitance.

4) Source voltage: When the source voltage changes during mixed-mode simulation, the current that flows into the source will change according to the power supply voltage. We assume that the change of current near the ground voltage Vgnd and power supply voltage Vcc is linearly related to the change of voltage as shown in Equations (9) and (11). The source current of the ground and the power supply can be expressed in terms of this voltage drop as shown in Equations (10) and (12).

$$\frac{Vgnd0 - Vgnd}{I(Vgnd0,t) - I(Vgnd,t)} = \text{const} \equiv Rgnd \quad (9)$$

$$I(Vgnd,t) = I(Vgnd0,t) - \frac{Vgnd0 - Vgnd}{Rgnd}\,, \quad (10)$$

where

Vgnd0 is the ground voltage when the source current model parameters were extracted,
Vgnd is the ground voltage when mixed-mode simulation is processed, and
I(Vgnd0,t) is the source current when the source current model parameters were extracted.

$$\frac{Vcc0 - Vcc}{I(Vcc0,t) - I(Vcc,t)} = \text{const} \equiv Rvcc \quad (11)$$

$$I(Vcc,t) = I(Vcc0,t) - \frac{Vcc0 - Vcc}{Rvcc}\,, \quad (12)$$

where

Vcc0 is the power supply voltage when the source current model parameters were extracted,
Vcc is the power supply voltage when mixed-mode simulation is processed, and
I(Vcc0,t) is the source current when the source current model parameters were extracted.

Equation (10) and (12) can be expressed using a interface circuit shown in Fig. 5, and the method for calculating the resistance values is described in the next section.

The parameters of the triangular source current model are extracted for only the basic gates, and when mixed-mode simulation is performed the source currents of each gate will be adjusted and calculated as follows:

$$\text{Ipeak} = \frac{W \cdot L0}{W0 \cdot L} \text{Ipeak0} \tag{13}$$

$$\text{Tend} = \frac{2(\text{Vcc} - \text{Vgnd})\text{Cld}}{\text{Ipeak}} - \text{Tstart} \tag{14}$$

IV. Source Current Model Parameter Extraction

The parameter extraction system consists of a circuit simulator and a parameter extractor. The input data needed for parameter extraction are the transistor level netlist of logic gates, the load capacitance equivalent to the capacitance due to gate fanout, and the input signal with the standard rise time and fall time of the gate. Circuit simulation is then performed and the source current model parameters will be extracted from the simulated current waveform. When extracting the parameters from the waveform, the following extraction conditions are specified (Fig. 6).

1) Current threshold: The threshold of the current is determined by specifying some proportion of the peak current or a certain current value. The source current model is obtained by drawing two lines from the peak current and the points crossing the threshold.
2) Logical threshold: Output voltage of the gate at which the logical value is determined to be high or low. The time at which the voltage reaches the threshold voltage is regarded as the event time of the gate.

The model parameters for basic gates will be extracted, and the source current of the individual gates will be adjusted in the current calculator of the mixed-mode simulator. To adjust the source current during mixed-mode simulation, extra model parameters need to be extracted.

To adjust the source current when the voltage of the power supply changes during mixed-mode simulation, the resistance value of the interface circuit is needed. This can be determined by extracting the peak current at two different source voltages.

$$R = \frac{\text{Vcc1} - \text{Vcc2}}{\text{Ipeak(Vcc1)} - \text{Ipeak(Vcc2)}}\ , \tag{15}$$

where

Vcc1 and Vcc2 are the different power supply voltages, and
Ipeak (Vcc1) and Ipeak (Vcc2) are the current peaks when the power supply voltage is Vcc1 and Vcc2.

To adjust the source current for different transistor sizes or load capacitance, the following parameters of the gates are needed:

1) WN0 (WP0): The channel width of the NMOS (PMOS) transistor
2) LN0 (LP0): The channel length of the NMOS (PMOS) transistor
3) Cld0: The equivalent load capacitance

V. Results of Voltage Fluctuation Analysis

We performed two kinds of simulations using a memory circuit that includes a power supply network. The first simulation was performed using part of the memory circuit and the results were compared to results obtained using a conventional circuit simulator. We simulated only the address buffer so that the conventional circuit simulator could run within a reasonable length of time. The address buffer of the memory circuit consisting of 2,356 transistors was analyzed -- simulating 150 transistors at the circuit level and 678 gates at the gate level -- with a maximum time step of 0.1 ns and transient analysis time of 100 ns. Model parameters for 22 gates were extracted. Simulations were performed by circuit simulation and by mixed-mode simulation with and without voltage fluctuation analysis.

Fig. 7 shows the current and voltage waveforms of a power supply network. The peak of the voltage drop and the time of the peak in these three simulations are listed in Table 1. We found that the differences between the maximum voltage fluctuations calculated by the mixed-mode simulations and those calculated solely by circuit simulation are within 20%.

Table 2 lists the performance of the circuit simulator and the mixed-mode simulator. The simulation using the proposed method took 2.2 CPU minutes on an HP9000/735 workstation, whereas the circuit simulator took 20.5 minutes. That is the proposed simulator was almost ten times as fast as the SPICE-like circuit simulator.

The second simulation analyzed the entire memory circuit, consisting of about 36,000 transistors -- simulating 4,896 transistors at the circuit level and 7,904 gates at the gate level -- with a maximum time step of 0.1 ns and a transient analysis time of 50 ns. Voltage fluctuation was analyzed within 75 minutes.

VI. Conclusion

We have presented an efficient logic/circuit mixed-mode simulator that can simulate voltage fluctuations in the power supply network of an entire VLSI chip. The current flowing into the power supply is calculated when an event occur in the logic simulator. When the circuit simulator calculates circuit behavior, the power supply current is calculated and included in the circuit simulation. This mixed-mode simulator uses a triangular source current model that incorporates the source current of the CMOS logic gates. This model requires the parameters of only the basic gates to be extracted.

The differences between maximum voltage fluctuations calculated by mixed-mode simulations and those calculated solely by circuit simulation were within 20%, and the mixed-mode simulation was almost ten times as fast as circuit simulation. An entire MOS memory chip (36,000 transistors) can be simulated on an HP9000/735 within 75 minutes while

considering the voltage fluctuation of the power supply network, thus demonstrating the feasibility of these simulations.

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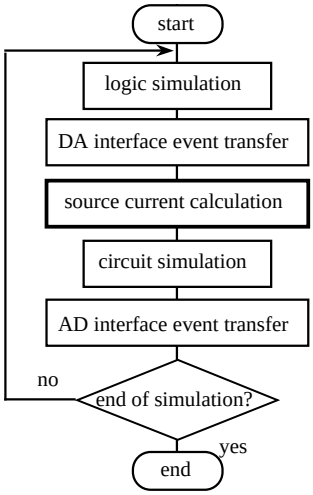
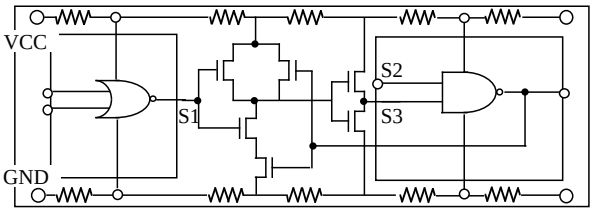
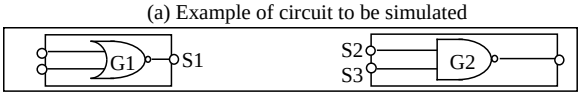


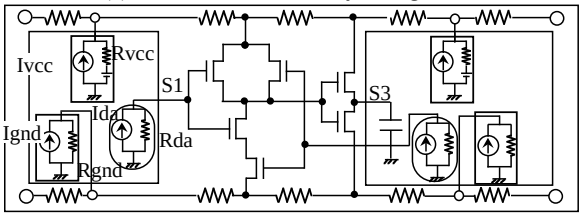
Fig. 1. Flow of the voltage fluctuation analysis.



(a) Example of circuit to be simulated



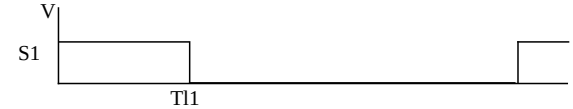
(b) Portion to be simulated by the logic simulator



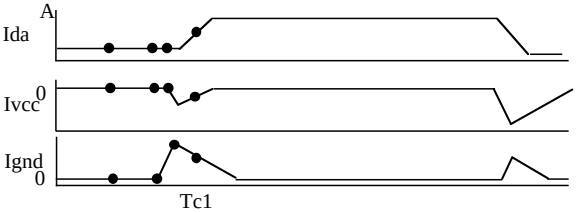
Current sources used to input the currents flowing into the power supply networks created by logic events of G1 and G2

Current sources used to input the signal of logic events

(c) Portion to be simulated by the circuit simulator

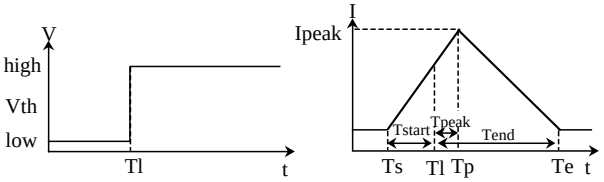


(d) Output of the NOR gate



(e) Input current of the circuit simulator

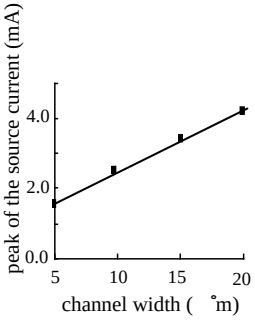
Fig. 2. Example circuit used for mixed-mode simulation.



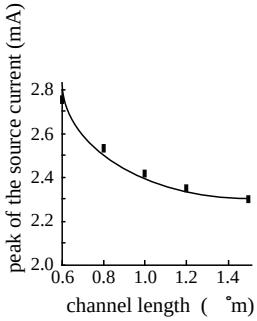
(a) Logical event

(b) Waveform of the triangular source current model

Fig. 3. Source current model.

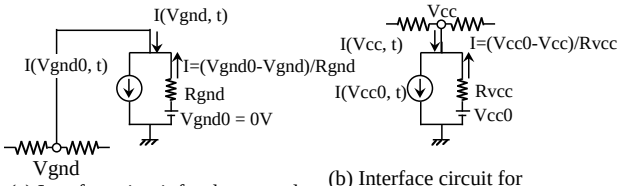


(a) Source current when the channel width of the MOS transistor has been changed



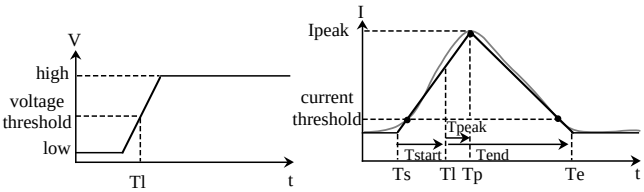
(b) Source current when the channel length of the MOS transistor has been changed

Fig. 4. Source current of an inverter.



(a) Interface circuit for the ground (b) Interface circuit for the power supply

Fig. 5. Interface circuit for the source current.



(a) Logical event (b) Current waveform created by the extractor

Fig. 6. Triangular source current extraction.

TABLE I.
ACCURACY OF THE MIXED-MODE SIMULATOR.

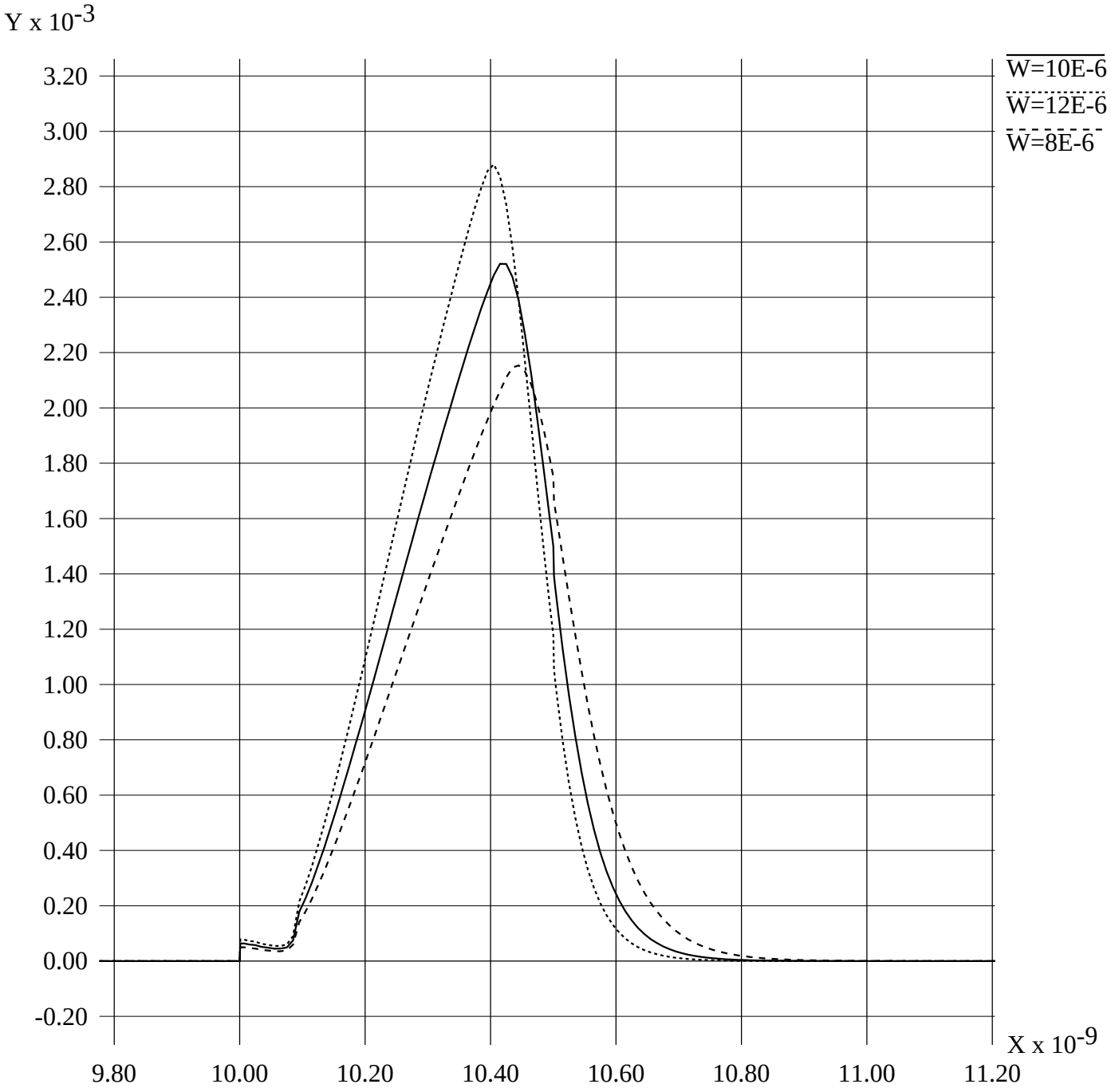
		Circuit simulation(a)	Mixed-mode simulation (*with* voltage fluctuation analysis) (b)	Difference (a) - (b)	Relative error (|(a)-(b)|/(a)
Peak of source current (mA)	VCC	123.8	123.6	0.2	0.16%
		104.2	118.0	-13.8	13.2%
	GND	48.2	53.7	-5.5	11.4%
		40.0	46.2	-6.2	15.5%
Peak of voltage fluctuation (mV)	VCC	236.7	227.8	-8.9	3.8%
		196.8	235.2	-38.4	19.5%
	GND	188.0	188.0	0.0	0.0%
		158.0	170.0	-12.0	7.6%
Time of the fluctuation peak (ns)	VCC	23.78	23.65	-0.13	-
		73.90	73.65	-0.25	-
	GND	23.77	23.65	-0.12	-
		73.91	74.00	-0.09	-

TABLE II.
SIMULATOR PERFORMANCE.

	Circuit simulation(a)	Mixed-mode simulation (*with* voltage fluctuation analysis) (b)	Mixed-mode simulation (*without* voltage fluctuation analysis) (c)
Number of elements (transistors)	2497 (2356)	667 (150)	334 (150)
Number of gates	-	678	678
CPU time (CPU time ratio)	20.5 min	2.2 min ((a)/(b): 9.3)	1.0 min ((a)/(c): 20.5)
Analysis point of the circuit simulator	1421	1054	1048
Number of iterations	5194	3039	1062
Number of logic events	-	2885	2885

Simulated up to 100ns, on an HP9000/735 Workstation

X Graph


Y x 10-3
3.20
3.00
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9.80
10.00
10.20
10.40
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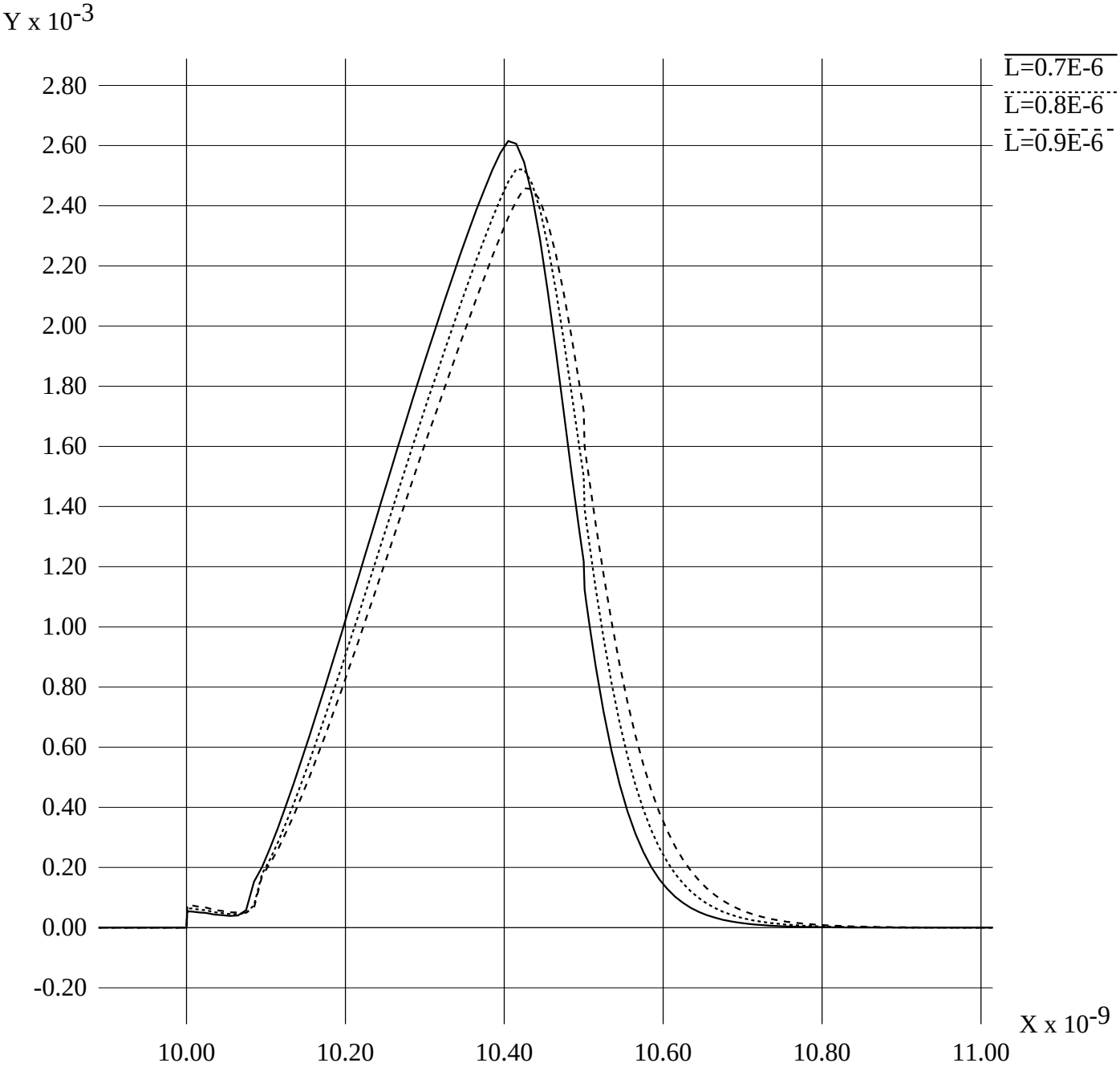
10.80
11.00
11.20
X x 10-9
W=10E-6
W=12E-6
W=8E-6

X Graph


Y x 10-3
2.80
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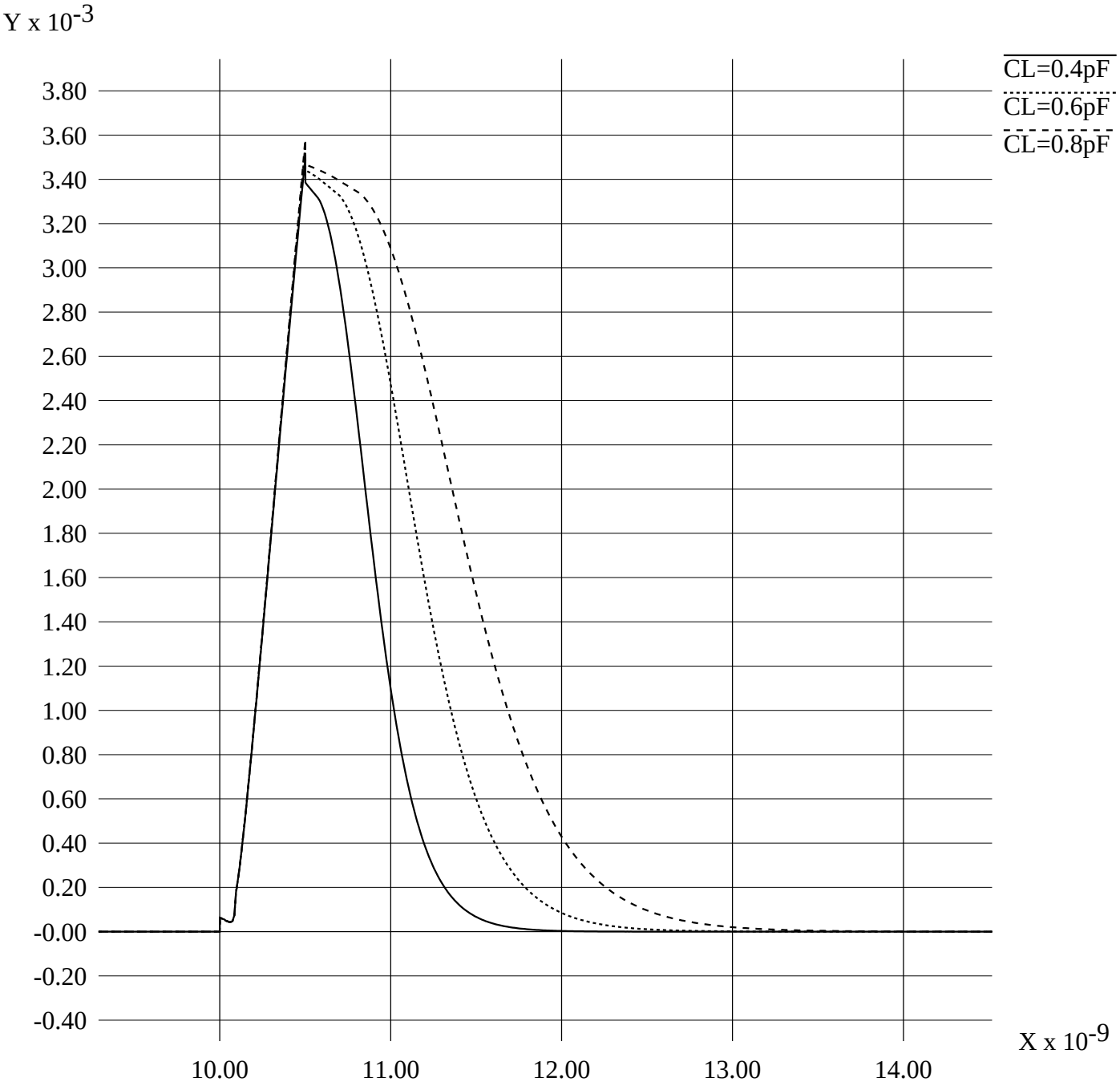
10.00
10.20
10.40
10.60
10.80
11.00
X x 10-9
L=0.7E-6
L=0.8E-6
L=0.9E-6

X Graph


Y x 10-3
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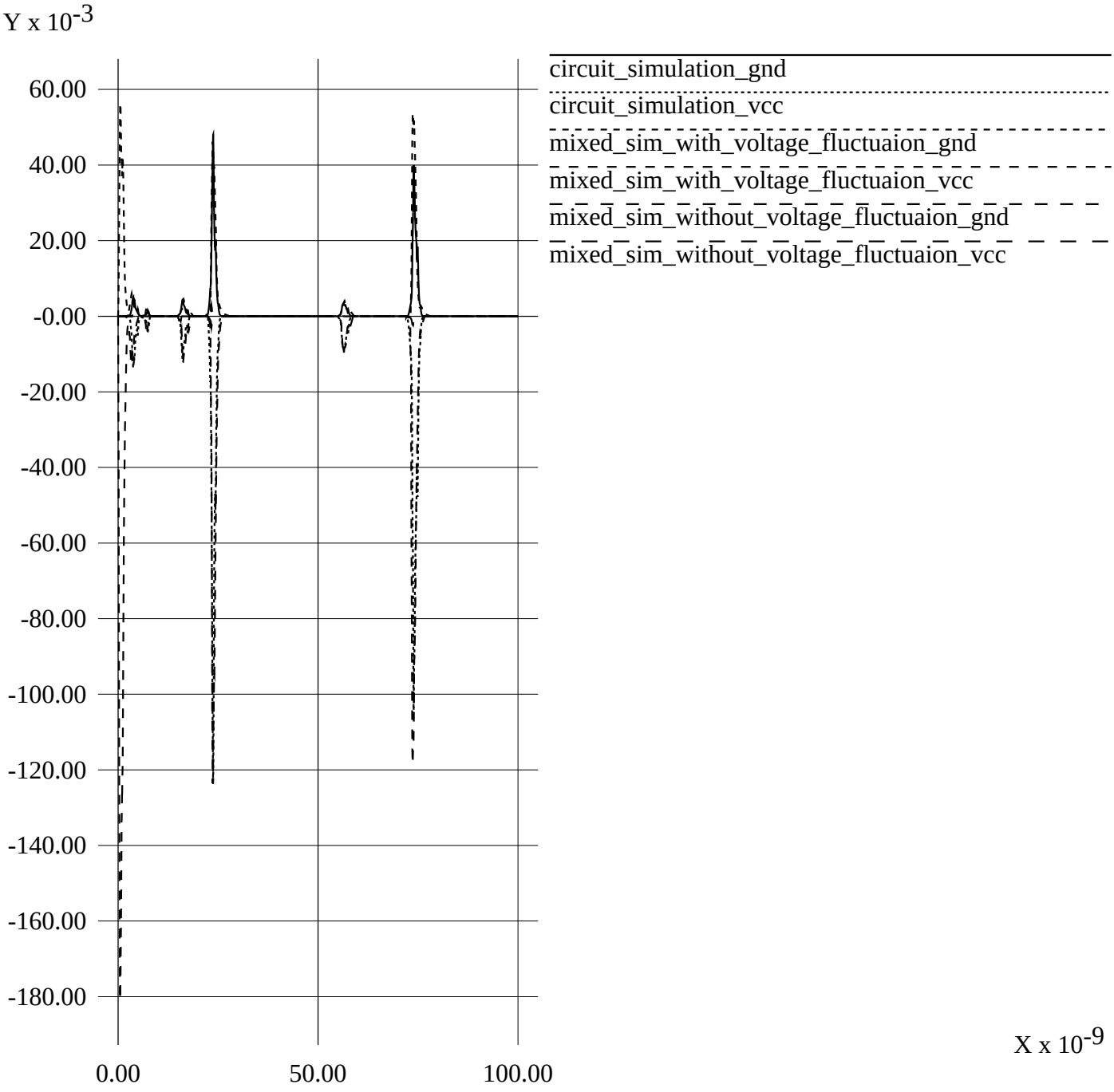
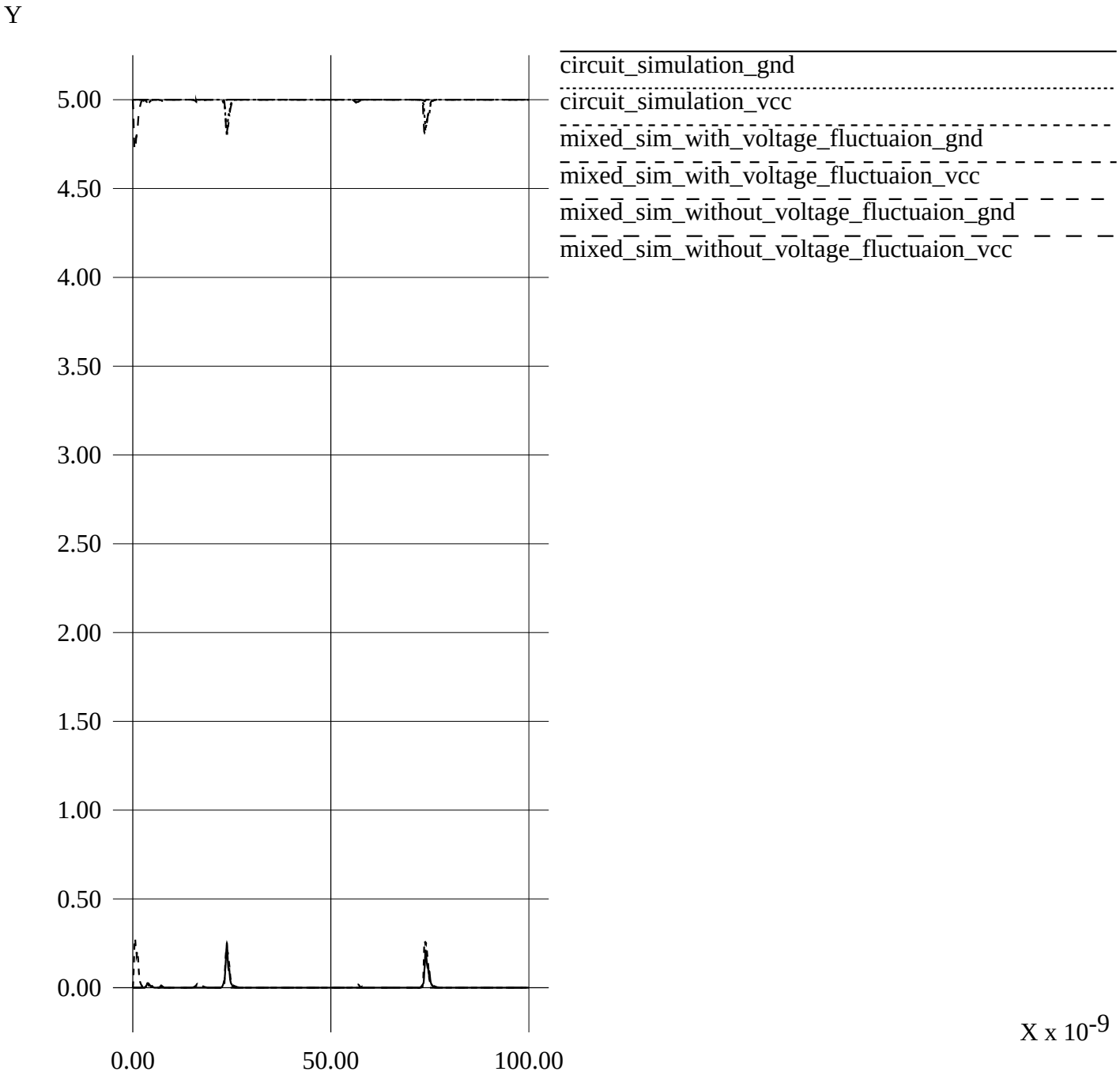
1.00
0.80
0.60
0.40
0.20
-0.00
-0.20
-0.40
10.00
11.00
12.00
13.00
14.00
X x 10-9
CL=0.4pF
CL=0.6pF
CL=0.8pF

X Graph


Y x 10-3
60.00
40.00
20.00
-0.00
-20.00
-40.00
-60.00
-80.00
-100.00
-120.00
-140.00
-160.00
-180.00
0.00
50.00
100.00
X x 10-9
circuit_simulation_gnd
circuit_simulation_vcc
mixed_sim_with_voltage_fluctuaion_gnd
mixed_sim_with_voltage_fluctuaion_vcc
mixed_sim_without_voltage_fluctuaion_gnd
mixed_sim_without_voltage_fluctuaion_vcc

X Graph


Y
5.00
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
0.00
50.00
100.00
X x 10-9
circuit_simulation_gnd
circuit_simulation_vcc
mixed_sim_with_voltage_fluctuaion_gnd
mixed_sim_with_voltage_fluctuaion_vcc
mixed_sim_without_voltage_fluctuaion_gnd
mixed_sim_without_voltage_fluctuaion_vcc