A New and Accurate Interconnection Delay Time Evaluation in a general Tree–Type Network.

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ABSTRACT

In all recent technologies the delay caused by interconnection wires is essential in the evaluation of the switching speed of integrated structures. Completely wrong results, would result if this were neglected. By considering a distributed RC network to model the interconnection lines, we proposed a new analytical delay time expression for a general tree type network, with full incorporation of technology design parameters. A computationally simple technique is presented and comparisons with HSPICE simulation results show the accuracy of the developed model in timing verification.

1. Introduction

In MOS integrated circuits, a given logic gate may drive several gates, some of them through long wires whose distributed resistance and capacitance may not be negligible. As device dimensions are scaled down, the interconnection delay among logic gates becomes as important as the logic–gate delay in determining the overall speed performance of a VLSI chip [1,2,3].
The delays caused by interconnection wires are then essential in the evaluation of the switching speed of integrated structures and disregarding them would give completely incorrect results.
Modeling digital MOS circuits by RC networks has become a well accepted practice for estimating delays. In 1981, Penfield and Rubinstein [4,5] proposed a method to bound the waveforms of nodes in an RC tree network. Later, Horowitz [6] extended this method to include both effects of slow inputs and non linearity of MOS transistors. It yields only a reasonable approximation to the true delay.
Recently, many interconnection delay models have been developed [7,8,9]. However, there are some problems to be solved. The first problem is that the effect of a logic gate on the interconnection delay and the effect of interconnection on the gate delay were not characterized appropriately [10,11,12]. Modeling these effects separately or modeling a logic gate by a single linear RC circuit may lead to significant error or intolerable inaccuracy in high performance design.
For our purposes, only the delay values are of interest, not the detailed waveforms. It has been generally recognize that, in CMOS structures, delay of gates can be accurately described through design parameters such as : technology, size of active components and parasitic capacitances [13, 14].
We propose to extend this approach to resistive loading terms in order to accurately characterize interconnection delays, differentiating purely capacitive from mixed resistive and capacitive contributions.
Our goal is to develop a simple but accurate analytic model with full incorporation of technology and design parameters. We define the contribution of line characteristics, its length, load and controling gate.
We first study how to efficiently compute signal delays on a single interconnection between two inverters.
Then we present a computationally simple technique for finding the worst case delay in an RC tree network and simple upper and lower bounds for the other delays associated with each output. An algorithm for calculating delays of all nodes is presented.
Through extensive comparisons with SPICE simulation results, it is shown that the maximum relative error of the developed model is below 12%. A circuit example is also presented to demonstrate the applications of the developed model in timing verification.

2. Analytical expression for a single interconnection

The interconnection line is usually modeled by an RC π–type model where Ri is the total wire resistance and Ci the total wire capacitance.

In preceding work [13] we showed that timing real responses of an inverter could be easily obtained through a linear combination of step responses. Each step response was evaluated through real design parameters involving speed characteristics of the process (τ_{st}), load and strength of the switching transistors, expressed as a ratio of capacitances, such as [14, 15] :

$$T_{hlp1} = \tau_{st} \frac{C_L + Ci}{2\ C_{Ns}} \qquad (1)$$

here the interconnection is modeled at the first order by its capacitance Ci. C_{Ns} represents the gate capacitance of the N switching transistor and C_L the load capacitance.

If like in the Elmore delay model, we model the inverter by

an equivalent resistor Rinv, the exact mathematical solution of the pulse delay between input and output at Vcc/2 is given by :

$$T_{hlp1} = \ln(2)\ \ Rinv\ (Ci + C_L) \qquad (2)$$

We now model the interconnection by a π–type Ri Ci circuit where Ri and Ci are the total interconnection resistance and total capacitance respectively, (Fig. 1a). The resistance Ri introduces an extra term which can be written as :

$$T_{hlp2} = \tau_{st}.\frac{C_L + Ci}{2\ C_{Ns}} + X \qquad (3)$$

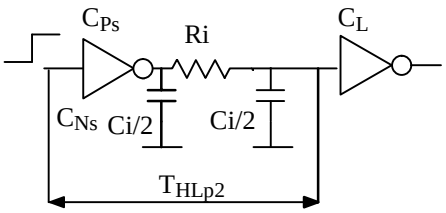


Fig.1a : Inverter with the interconnection modeled by a π model.

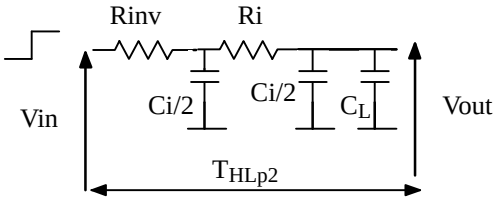


Fig.1b : Total RC equivalence representation.

We now replace the inverter by its equivalent resistor Rinv, and the interconnection by a π–type Ri Ci circuit (Fig. 1b). The exact calculation of the signal delay through such a network is difficult. After some simplification, the step response of this cell, evaluated at half swing of the output voltage (Vcc/2) is given by :

$$T_{hlp2} = \ln(2)\ \left(Rinv(Ci + C_L) + Ri(Ci/2 + C_L)\right) \qquad (4)$$

Combining eq. 1, 2, 3 and 4 gives an analytical expression for the total delay including that which results from the interconnection :

$$T_{hlp2} = \tau_{st}\frac{Ci + C_L}{2C_{Ns}} + \ln(2)\ \ Ri\ \left(\frac{Ci}{2} + C_L\right) \qquad (5)$$

3. Analytical expression for two divergence branches

To begin this study, we evaluate the delays of two divergence branches circuit (Figure 2), which we then compare with SPICE simulation results.

The propagation delay introduced between the input and output at Vcc/2 is given by using the circuit described in figure 2.

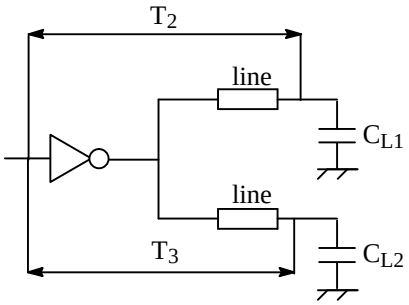
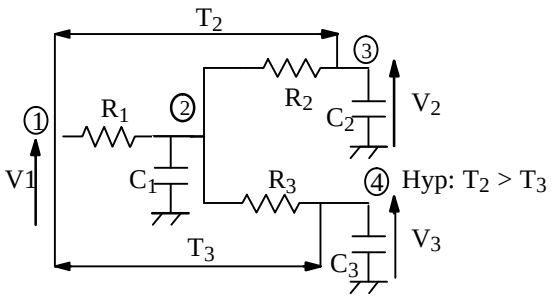


Fig.2 : Circuit including 2 divergence branches.

We now replace the inverter by its equivalent resistor (R_1) and the interconnection lines by a π –type RC circuit (Figure 3).



with C_1,C_2 and C_3 the sum of node capacities 2,3 and 4 respectively.

Fig.3 : RC equivalence representation to figure 3.

To accurately define the delays T_2 and T_3, we must first express the transfer functions $\frac{V_2}{V_1}$ and $\frac{V_3}{V_1}$. By application of nodes law and Laplace transform we can obtain the transfer functions which are of the third order. Afterwards, the difference delays cannot be found in closed form. Then, the solution of the transfer function can be obtained numerically.In order to obtain a delay T_2 greater than T_3, we give a value of R_2C_2 product superior to R_3C_3. The output node 3, equivalent to the critical delay of the circuit of figure 3, will reach the voltage $V_{cc}/2$ after all others nodes of the circuit. It is then possible to simplify its transfer function, after which we obtain the corresponding critical delay in the first order :

$$T_2 = \ln(2)\ \ [R_1(C_1 + C_2 + C_3) + R_2C_2] \qquad (6)$$

The output node 4 reaches the voltage of $V_{cc}/2$ before the output node 3. In a first approximation, the delay T_3 will be evaluated as the average between an upper bound defined in the same way as the critical way and an lower bound where we suppose that the output node 4 will reach the voltage $V_{cc}/2$ before the output node 3 has begun to be loaded.
We will now go back to the initial circuit of figure 3 and R_2, R_3, C_1, C_2 and C_3 by its equivalent interconnection values, we has obtained the following equations :

$$T_2 = \frac{\tau_{stn}}{2C_N}(C_{i1} + C_{i2} + C_{L1} + C_{L2}) + \ln(2)\ R_{i1}\left(\frac{C_{i1}}{2} + C_{L1}\right) \qquad (7)$$

$$T_3 = \frac{\tau_{stn}}{2C_N}\left(\frac{3C_{i1}}{4} + C_{i2} + \frac{C_{L1}}{2} + C_{L2}\right) + \ln(2)\ R_{i2}\left(\frac{C_{i2}}{2} + C_{L2}\right) \qquad (8)$$

In table 1 we compare values of the delays calculated using the preceding equations to values obtained from Hspice for different line configurations and for different transistor widths and loads of switching inverters.

W_N = 4 µm W_P = 12 µm Polysilicon line				
Loads	Lenght of lines	Simulation (ps)	Calculation (ps)	Difference Form/ Sim
$C_{L1}=C_{L2}$ $= C_N+C_P$	L_1=200 µm L_2=100 µm	T_2=272 T_3=177	T_2=261 T_3=164	**–4%** **–7.3%**
	L_1=300 µm L_2=50 µm	T_2=377 T_3=167	T_2=365 T_3=148	**–3.2 %** **–11 %**
$C_{L1}=3C_{L2}$ $C_{L2}=C_N+C_P$	L_1=200 µm L_2=50 µm	T_2=463 T_3=143	T_2=472 T_3=158	**+2 %** **+10%**
W_N = 12 µm W_P = 36 µm				
$C_{L1}=C_{L2}$ $= C_N+C_P$	L_1=300 µm L_2=100 µm	T_2=550 T_3=211	T_2=551 T_3=207	**+0.2 %** **–1.9 %**

Table 1 : Comparison between the delay determined by calculation and simulation.

Table 1 shows the agreement obtained between calculated and simulated values for different sizes of switching inverters and lengths of line. These results allow us to validate the equations of the delays (7 and 8) in the cases where the logic gate drives the network.

Rubinstein, Penfield and Horowitz [5] proposed upper and lower bounds for the output waveform in response of an RC tree by an introducing three time constants. Our method, based an the only delays values is easier to use for a fast computationaly delay evaluation.

To obtain equivalent delays in all divergence branches Tsay [15] proposes to shift the divergence point of interconnections lines in order to equilibrate the different delays. From the preceding equations, another solution, that of the modification of the size of the load gate to obtain equal delays, would seem simpler.

In the particular case of the circuit illustrated in figure 2, we obtain equality between the delays T_2 and T_3 when equivalent capacity of the load gate is given by the following equation :

$$C_{L2} = \frac{R_{i1}}{R_{i2}}\left(\frac{C_{i1}}{2} + C_{L1}\right) - \frac{C_{i2}}{2} \qquad (9)$$

For the first and third cases of table 1, we obtain as new load to equal the delays T_2, T_3 the respective values :

$$C_{L2} = 100\ fF = 2.85(C_N+C_P)$$
$$C_{L2} = 497\ fF = 14.2(C_N+C_P)$$

4. Generalization to a several divergence branches circuit

In the preceding chapter we defined the delays in the case of two divergence branches, we will now generalize our method to the RC tree network.

A. Pulse delay evaluation in several divergence branches

The critical delay will be evaluated as the output delay which last reaches the half swing of the output voltage (Vcc/2). The other delays will be evaluated by an average between the upper and lower bounds.

Our method of delay evaluation for a several interconnection lines circuit is laid out in the following steps :

– numbering each RC network node in increasing order beginning by the driver gate output,

– calculating the equivalent capacitances for each circuit node,

– defining the resistance set which belongs to the path between nodes e end j :
Y(e,j) where e is the output node of the driver and j is a node of the circuit,

– defining the crossing order of different circuit nodes for a reference voltage :

$$X(j) = \sum_{u=(kk')/u\in \text{path from e to j}} \left[R_u \left(\sum_{l\in[Des\ (k')+k']} C_l \right) \right]$$

where :
- kk' are the numbers of network resistance connections (k'>k),
- u is an arc defined by the kk' connections and belongs to the Y(e,j),
- l is the set of nodes including k' and its descendants from a topology point of view.

At this point, it is necessary to define the X(j) for divergence nodes of the RC network and input nodes of the different load gates.

– Classing the X(j) in decreasing order :
  – the X(j) maximal value will correspond to the maximum delay of the circuit,
  – the X(j) minimal value will correspond to the minimum delay of the circuit.

– Critical delay calculation : the delay of the output nodes will reach the voltage Vcc/2 after all other circuit nodes.

$$T_{[(e-1)\ ,\ s]p} = \frac{\tau_{stn}}{2C_N} \sum_{k=e}^{y} C_k + \ln(2)\ X(s) \qquad (10)$$

where :
– s is the input node of the load gate which is the last to reach Vcc/2,
– y is the highest node of the network RC,
– (e–1) is the input node of the driver gate.

– Calculation of the delays below the critical delay. These delays are defined by the average between the upper and lower bounds :

$$T_{[(e-1)\ ,\ s]sup} = \frac{\tau_{stn}}{2C_N} \sum_{k=e}^{y} C_k + \ln(2)\ X(s) \qquad (11)$$

$$T_{[(e-1)\ ,\ s]inf} = \frac{\tau_{stn}}{2C_N} \sum_{h\in M} C_h + \ln(2)\ X'(s) \qquad (12)$$

where :
– s is the input node of the different load gates, except that of the output node, corresponding to the critical delay,
– M is the set of nodes of the network RC where the X(j) values are below or equal to the values of the output node considered(X(s))

$$X'(s) = \sum_{u=(kk')/u\in \text{path from e to j}} \left[R_u \left(\sum_{l\in[Des\ (k')+k']} C_l - \sum_{m\in X(Des(k'))>X(j)} C_m \right) \right]$$

where m is the set of nodes whose descending value X(j) is superior to values of the considered node X(j).

In a first approximation, the delay $T_{[(e-1)\ ,\ s]}$ will be calculated as the average between the equations 11 and 12 as :

$$T_{[(e-1)\ ,\ s]moy} = \frac{T_{[(e-1)\ ,\ s]sup} + T_{[(e-1)\ ,\ s]inf}}{2} \qquad (13)$$

B. Validations

In table 2, we compare the values of delays calculated using the equations 10, 11, 12, and 13 to values obtained from Hspice simulations for different length wires and different loads. The delays obtained from the RC tree network are represented in figure 4.

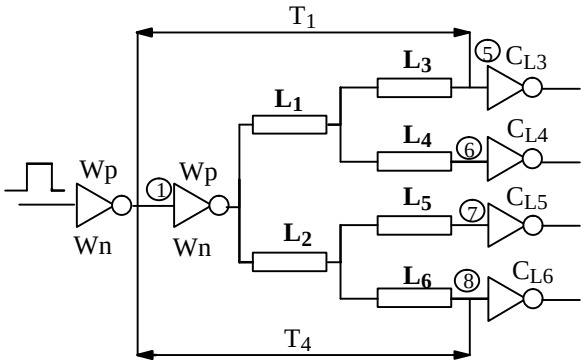


Fig.4 : RC tree network.

Within the context of this validation, the driver inverter of the RC tree network is not attacked by a step but by a real slope (output logic gate).
For this example, we shall not enumerate all the steps of the formulation but shall give directly the evaluation of the different circuit delays (Figure 4) (T_1 from T_4).

– T_1 is the delay between node 1 and node 5,
– T_2 is the delay between node 1 and node 6,
– T_3 is the delay between node 1 and node 7,
– T_4 is the delay between node 1 and node 8.

Polysilicon line Technology 1.5 µm Runit =15.625 Ω/µm Cunit =0.205 fF/µm			
Loads (fF)	Lengths	Simulation (ps)	Calculation (ps)
	Wn=4µm Wp=12µm		
C_{L3}=C_{L4} =C_{L5}=C_{L6} =35.33	L_1=L_2=L_3=L_4 =L_5 =L_6=50 µm	T_1=T_2=T_3 =T_4=282	T_1=T_2=T_3= T_4=299 **+6%**
	L_1=200 µm L_2=100 µm L_3=200 µm L_4=50 µm L_5=100 µm L_6=50 µm	T_1=726 T_2=571 T_3=395 T_4=353	T_1=741 **+2%** T_2=555 **-2.8%** T_3=411 **+4%** T_4=336 **-4.8%**
	L_1=300 µm L_2=100 µm L_3=200 µm L_4=50 µm L_5=300 µm L_6=150 µm	T_1=977 T_2=820 T_3=730 T_4=518	T_1=1013 **+4%** T_2=795 **-3%** T_3=723 **-1%** T_4=520 **+0.4%**
C_{L3}=35 C_{L4}=70 C_{L5}=105 C_{L6}=140	L_1=300 µm L_2=100 µm L_3=200 µm L_4=50 µm L_5=300 µm L_6=150 µm	T_1=1206 T_2=1075 T_3=1339 T_4=1046	T_1=1270 **+5%** T_2=1072 **-0.3%** T_3=1420 **+6%** T_4=1030 **–2%**

Metal 1 line Technology 1.5µm Runit =18.75e-3 Ω/µm Cunit =0.165 fF/µm Wn=16µm Wp=48µm			
$C_{L3}=C_{L4}$ $=C_{L5}=C_{L6}$ =175	L_1=1 cm L_2=7 mm L_3=2 cm L_4=5 mm L_5=1 cm L_6=3 mm	T_1=3540 T_2=2870 T_3=2370 T_4=2200	T_1=3670 **+3.6%** T_2=2890 **+0.7%** T_3=2250 **-5%** T_4=2000 **-9%**

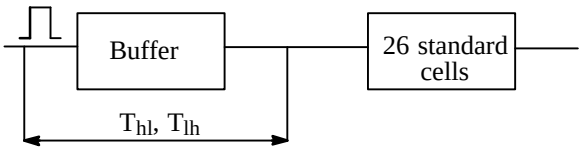
Table 2 : Validation of delays obtained for polysilicon and metal lines.

As shown in table 2, the agreement obtained between calculated and simulated values (the error is less than 10%) confirms the validity of the delay expression within the RC tree network.

5. Application to industrial circuit

Having dealt with these different examples we shall now apply the delay calculations obtained in the divergence branches to a real circuit built with 0.7 micron technology with two possible metallization levels. This circuit constitutes a buffer which attacks identical standard cells through the intermediary of an RC tree network. Each of these lines is modeled by an RC–π–type network whose resistance and capacitance values have been evaluated by electric extraction. This circuit includes 79 RC networks and 26 output nodes corresponding to identical standard cells represented by their equivalent capacitances.

First of all, we shall evaluate this circuit delay without taking into consideration the interconnection lines.



Delays	Calculation	Simulation
T_{hl}	0.482 ns	0.497 ns
T_{lh}	0.512 ns	0.525 ns

Fig. 5 : Evaluation of delays without interconnection lines.

We calculate all the circuit delays between the buffer input and each of the output capacitances.

	Technology 0.7 micron		
Delay T(node)	Calculation (ns)	Simulation (ns)	Difference %
T(51) hl lh	1.282 1.415	1.277 1.387	+ 0.43 + 2
T(4) hl lh	1.267 1.398	1.276 1.387	– 0.6 + 0.82
T(79) hl lh	1.234 1.361	1.274 1.385	– 3.1 – 1.7
T(36) hl lh	1.217 1.342	1.273 1.384	– 4.4 – 3
T(23) hl lh	1.197 1.321	1.273 1.383	– 6 – 4
T(57) hl lh	1.163 1.283	1.264 1.376	– 8 – 6.76
T(71) hl lh	1.135 1.253	1.258 1.369	– 9.8 – 8.47
T(28) hl lh	1.114 1.226	1.252 1.364	– 11 – 10.1
T(64) hl lh	1.075 1.19	1.225 1.336	– 12.2 – 10.9
T(60) hl lh	0.8 0.89	0.817 0.93	– 2.1 – 4.3
T(30) hl lh	0.795 0.885	0.807 0.92	– 1.5 – 3.8
T(10) hl lh	0.745 0.828	0.738 0.846	+ 0.9 – 2.13
T(81) hl lh	0.714 0.793	0.7 0.805	+ 2 – 1.5
T(58) hl lh	0.674 0.75	0.633 0.73	+ 6.5 + 2.7
T(16) hl lh	0.656 0.728	0.62 0.714	+ 5.8 + 2
T(19) hl lh	0.63 0.698	0.59 0.681	+ 6.18 + 2.5
T(42) hl lh	0.624 0.688	0.59 0.679	+ 5.7 + 1.3
T(69) hl lh	0.616 0.67	0.589 0.679	+ 4.6 – 1.32
T(74) hl lh	0.608 0.67	0.587 0.678	+ 3.6 – 1.2
T(24) hl lh	0.595 0.654	0.574 0.663	+ 3.6 – 1.35
T(50) hl lh	0.59 0.645	0.573 0.662	+ 2.9 – 2.6
T(35) hl lh	0.575 0.627	0.561 0.648	+ 2.5 – 3.2
T(70) hl lh	0.556 0.605	0.536 0.619	+ 3.7 – 2.26

T(14) hl lh	0.541 0.599	0.535 0.619	+ 1.12 – 3.23
T(66) hl lh	0.522 0.568	0.487 0.564	+ 7.18 + 0.7
T(7) hl lh	0.518 0.562	0.486 0.564	+ 6.6 – 0.35

Table 3 : Comparison of delays determined by calculation or simulation.

As shown in table 3, the correlation between calculated and simulated values is good (error less than 11%). In the critical delay (most often used to characterize a circuit), the difference between calculation and simulation is about 2%.

The results obtained with an industrial circuit (table 3) allow the validation of the equations defined in the RC tree network. By including interconnection lines the circuit delay is increased. In fact, in the event of any critical delay (T_{51}), the total delay (including the interconnection lines) is about two and half times the delay without the interconnection lines. So, to calculate an accurate delay of a circuit, it is absolutely necessary to consider the additional delay resulting from the interconnection lines.

Moreover, this calculation decreases the CPU delay compared with an electric simulation (in which the CPU delay depends on the number of nodes), and will be easily included in a timing simulator, like PATH–RUNNER [16].

6. Conclusion

We defined an analytical expression to evaluate the delays in RC tree networks. This formulation can be applied to any kind of circuit including divergence branches, and used in any type of technology.

The delays calculated with this formulation were in very close agreement with those derived from Hspice electrical simulations. The results we obtained show that we need to take into account interconnection lines in order to evaluate the total circuit delay.

The facility with which our analytical expression can be applied makes it suitable to be incorporated in a temporal simulator. Moreover it could be used to define rules to minimize the contribution of interconnection delays to the total circuit delays.

REFERENCES

[1] K.C. Saraswat, F.Mohammedi, " Effect of scaling of interconnections on the time delay of VLSI circuits ", IEEE Trans. Electron Devices, vol. ED–29, Apr.1982.

[2] C.Y. Wu, M.C.Shiau, " A new interconnection delay model considering the effects of short–channel logic gates ", in Proc. IEEE Int. Symp. Circuits Syst., pp. 2847–2850, June 1988.

[3] M.C. Shiau, C.Y. Wu, " The signal delay in interconnection lines considering the effects of small–geometry CMOS inverters ", IEEE Trans. Circuits Syst., vol 37, pp. 420–425, Mar.1990.

[4] P.Penfield, J.Rubinstein, "Signal Delay in RC Tree Networks", IEEE 18th Design Automation Conference, pp 613–617, June 1981.

[5] J.Rubinstein, P.Penfield and M.A.Horowitz "Signal delay in RC tree networks", IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems, CAD–2, pp 202-211, July 1983.

[6] M.Horowitz, "Timing Models for MOS Pass networks", IEEE International Symposium on Circuits and Systems proceedings, pp 198–201, 1983.

[7] C. Y. Wu, M.C. Shiau, " Delay models and speed improvement techniques for RC tree Interconnections among small–geometry CMOS inverters ", IEEE J. of Solid–State Circuits, vol. 25, nº5, Oct.1990.

[8] M. Nekili, Y. Savaria, " Optimal methods of driving interconnections in VLSI circuits ", in Proc. IEEE Int. Symposium on Circuits and Systems, San Diego, pp.21–24, May 1992.

[9] J. L. Wyatt, Jr. and Q. YU, " Signal delay in RC meshes, trees and lines ", in Proc. IEEE Int. Conf. Computer Aided Design, Santa Clara, CA, pp. 15–17, Nov.1984.

[10] J.L. Wyatt, Jr., " Signal delay in RC mesh networks ", IEEE Trans.Circuits Syst., vol. CAS–32, pp. 507–510, May 1985.

[11] Q. Yu, J.L. Wyatt, Jr., C. Zukowski, H.N. Tan, P. O'Brien, " Improved bounds on signal delay in linear RC models for MOS interconnect ", in Proc. IEEE int. Symp. Circuits Syst., (Kyoto, Japan), pp. 903–906, June 1985.

[12] M. Passlack, M. Uhle and H. Elschner, " Analysis of propagation delays in high–speed VLSI circuits using a distributed line model ", IEEE Trans. on Computer–Aided Design, vol. 9 nº8, Aug. 1990.

[13] D. Deschacht, M. Robert, D. Auvergne " Explicit formulation of delays on CMOS data paths," IEEE J. Solid–State Circuits, Vol. 23, n 5, pp. 1257–1264, Oct. 1988.

[14] D. Deschacht, M. Robert, D. Auvergne "Synchronous mode modeling of delay time in CMOS structures", IEEE J. Solid–State Circuits, vol. 26, pp 789–795, May 1991.

[15] R.S. Tsay " An Exact Zero–Skew Routing Algorithm " IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol.12, n3, pp. 242–249, February 1993.

[16] D. Deschacht, M. Robert, N. Azemard–Crestani, D. Auvergne " Post–Layout Timing Simulation of CMOS Circuits ", IEEE Trans. on Computer–Aided Design, vol.12, Nº8, pp 1170–1177, August 1993.