Future Direction of Synthesizability and Interoperability of HDL's

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One of the key issues in EDA (Electronic Design Automation) technologies is the improvement of design productivity and quality of electronic systems including VLSI's. There are several major HDL's (Hardware Description Languages), including VHDL, Verilog-HDL, UDL/I and SFL, being used by many system and VLSI designers in order to achieve this goal. However, many of these designers have been more or less suffered from the incompatibility of these HDL's and their processing systems. Synthesizable model standardization that covers various HDL's is the key issue to the interoperability among these HDL's. This session gives a tutorial on the synthesizability and interoperability among HDL's, then we will discuss future direction of these issues.

Panel Members:

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