

# BIST with Negligible Aliasing through Random Cover Circuits

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**Abstract—** In this paper, a new modified BIST structure is investigated. The output of the MISA is monitored during the test by an error detection circuit which is composed of two simple cover circuits. To simplify the cover construction, the cover circuits are randomly chosen to be active for some of the outputs of the MISA. Thus, a time-consuming fault simulation can be completely avoided. The overhead for the cover circuits is determined for several of the ISCAS'85 and Berkeley benchmark circuits. These simulation experiments show that a significant reduction of the aliasing probability can be achieved, confirming and far surpassing theoretically predicted improvements. Moreover, this improvement can be achieved at a nearly negligible cost in additional hardware.

## I. INTRODUCTION

In a conventional built-in self-test (BIST) structure, a sequence  $x(0), \dots, x(T-1)$  of inputs provided by a test input generator (TIG) is applied to the circuit under test (CUT). The corresponding output sequence  $y(0), \dots, y(T-1)$  is processed by a multiple-input signature analyser (MISA) with initial state  $z(0)$ . The final state vector  $z(T)$  of the MISA after  $y(0), \dots, y(T-1)$  have been processed is called the signature. The actual signature is compared to the expected one; a fault is indicated in the CUT if the two signatures are not equal.

If the CUT is erroneous and the actual signature is equal to the expected signature, aliasing occurs. Several different methods have been suggested for reducing the probability of aliasing [1, 2, 3, 4, 5]. All of these proposals use the outputs of the MISA — ignored in the common BIST realizations — to reduce the probability of aliasing.

In [3] it is proposed to monitor a single component — or some components — of the signature analyser by a simple error detection circuit composed of a 1-cover circuit and a 0-cover circuit for a corresponding partially-defined Boolean function. The cover circuits need to detect only those incorrect outputs of the MISA that are caused by

faults leading to the correct signature. Moreover, the cover circuits need to detect only a single incorrect bit in such a faulty output sequence. Hence, the cover circuits will have a very large number of don't-care conditions and, hence, have very small realizations.

Determining the cover circuits as specified in [3], however, requires very extensive fault simulation. In this paper, we demonstrate how this time-consuming fault simulation can be avoided. Only the correct behaviour of the CUT for the input sequence  $x(0), \dots, x(T-1)$  and the correct output sequence of the MISA have to be determined. The cover circuits are made active at randomly chosen times for a given percentage of outputs of the MISA in test mode. While the complete cover circuits can guarantee that no aliasing will occur [3], the randomly chosen covers may incur a non-zero probability of aliasing. In this paper, we first determine the theoretical value of this probability. We then report experimental results obtained using the ISCAS'85 and Berkeley benchmark circuits. Simulations indicate a dramatic improvement of the aliasing probability at an extremely low cost in additional hardware.

This paper is structured as follows. In Section II, we review basic notions concerning fault models, BIST, and cover circuits. Then, in Section III, the construction algorithm for the proposed circuit is presented. The probability of aliasing for the proposed method is evaluated in Section IV. In Section V, the results of the experimental simulations are discussed. Section VI contains concluding remarks.

## II. BASIC NOTIONS AND NOTATION

In this section we establish some basic notation and review the required notions concerning conventional BIST and error detection by cover circuits.

In the sequel, let  $\mathbb{N}$  denote the set of positive integers and let  $\mathbb{B}$  denote the set  $\{0, 1\}$  of Boolean values. A bar above a symbol denotes negation and a bar below a symbol denotes a vector.

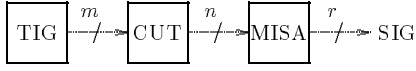


Fig. 1. Conventional BIST structure.

Let  $C$  be an arbitrary, but fixed combinational circuit with  $m$  inputs and  $n$  outputs, and let  $f = f_C : \mathbb{B}^m \rightarrow \mathbb{B}^n$  be the function realized by  $C$  if  $C$  is fault-free with  $m, n \in \mathbb{N}$ . Modulo 2 addition is denoted by  $\oplus$ , and  $\oplus$  is also used for sequences to denote componentwise modulo 2 addition.

#### A. Built-in Self-test

Fig. 1 shows the standard structure for BIST. A test input generator generates a test sequence of  $m$ -dimensional Boolean vectors, which is then applied to the CUT. The response of the CUT to the test is a sequence of  $n$ -dimensional output vectors, which is applied to an  $r$ -dimensional multi-input signature analyser for compression. Usually,  $r = n$ , although this is not a necessary condition. The final state of the MISA after the CUT output sequence has been applied is called the *signature* of the MISA.

Testing of the CUT is achieved by comparing the signature of the actual CUT to the signature which would result from the fault-free circuit under the same input sequence. If the two signatures are equal then the CUT is supposed to be fault-free. If, however, the signatures differ, the CUT is considered to be faulty. *Aliasing* or *error masking* occurs when a faulty CUT produces the same signature as the correct circuit. In this case, the testing procedure does not diagnose the CUT as faulty, and the faulty circuit remains undetected. Details regarding BIST can be found in [6, 7, 8].

#### B. Error Detection by Cover Circuits

In [9], error detection by cover circuits was introduced. The zero- and one-covers of a Boolean function  $g$  are defined as follows:

**Definition.** Let  $g, C_{0,g}, C_{1,g} : \mathbb{B}^k \rightarrow \mathbb{B}$  be  $k$ -ary Boolean functions with  $k \in \mathbb{N}$ .

- (a)  $C_{0,g}$  is a 0-cover of  $g$  if, for all  $x \in \mathbb{B}^k$ ,  $C_{0,g}(x) = 1$  implies  $g(x) = 0$ .
- (b)  $C_{1,g}$  is a 1-cover of  $g$  if, for all  $x \in \mathbb{B}^k$ ,  $C_{1,g}(x) = 1$  implies  $g(x) = 1$ .

A fault in the circuit implementing  $g$  is detected when  $C_{0,g}(x) \wedge g(x) = 1$  or  $C_{1,g}(x) \wedge \overline{g(x)} = 1$  for some input  $x \in \mathbb{B}^k$ . We say that  $C_{0,g}$  or  $C_{1,g}$  is *active* for  $x \in \mathbb{B}^k$  if  $C_{0,g}(x) = 1$  or  $C_{1,g}(x) = 1$ , respectively.

#### C. Error Detection Using BIST and Cover Circuits

We now combine BIST and cover circuits to reduce the probability of aliasing as shown in [3]. The cover circuits are constructed to monitor the one-dimensional output of the first component of the MISA. Let  $f : \mathbb{B}^m \rightarrow \mathbb{B}^n$  be the function realized by the CUT if it is fault-free. The TIG generates the input sequence — without repetitions —  $x(0), x(1), \dots, x(T-1)$  of  $m$ -dimensional vectors. For  $t = 0, \dots, T$ , let  $z(t | f)$  be the state vector of the MISA at time  $t$ , and let  $z_1(t | f)$  be its first component. From  $f$  one obtains a function  $g_f : \mathbb{B}^m \rightarrow \mathbb{B}$  constructed according to the following rules:

- (a)  $g_f(x)$  is defined for all  $x \in \{x(0), x(1), \dots, x(T-1)\}$ .
- (b) For  $x = x(t)$  let  $g_f(x) = z_1(t+1 | f)$ .

In general,  $g_f$  is a partial function; it is total if and only if  $T = 2^m$ . It is well-defined because the sequence  $x(0), x(1), \dots, x(T-1)$  contains no repetitions.

Fig. 2 shows the circuit which combines BIST with the cover circuits.  $M$  is a one-bit memory which is initialized to 0 before the test. The test input sequence generated by the TIG is applied to the CUT as well as to the covers  $C_{0,g_f}$  and  $C_{1,g_f}$ . The sequence  $y(0), y(1), \dots, y(T-1)$  of  $n$ -dimensional output vectors of the CUT is applied to the MISA, which is realized as a multi-input linear feedback shift register (MILFSR) with at least  $n$  stages. Let  $z(0), z(1), \dots, z(T)$  be the sequence of states of the MISA for the given CUT, that is,  $z(t+1)$  is the state obtained after the sequence  $y(0), y(1), \dots, y(t)$  has been applied to the MISA. At each step  $t$ , the cover circuits  $C_{0,g_f}$  and  $C_{1,g_f}$  are used to check  $z_1(t+1)$ , the first component of the current state vector of the MILFSR, if one of the covers is active at input  $t$ . The one-bit memory  $M$  is used to store the results from the comparisons of  $z_1(t+1)$  with  $C_{0,g_f}$  and  $C_{1,g_f}$ .

The circuit depicted in Fig. 2 detects faults in the CUT in one of two ways. If  $z(T | f) \neq z(T)$ , the BIST circuit detects a fault in the CUT. If  $z(T | f) = z(T)$ , the value of  $M$  is checked. If it is 1, a fault is detected in the CUT. In this case, an error has been detected by the covers in the sequence  $z_1(1), z_1(2), \dots, z_1(T)$ .

### III. COVER CIRCUIT CONSTRUCTION

In [3], it is shown how, in principle, the cover circuits  $C_{0,g_f}$  and  $C_{1,g_f}$  can be constructed deterministically for a given fault model. Zero aliasing can be achieved. Simulation results using the deterministic construction method are reported in [10]. With this method, however, the application of the test input sequence of length  $T$  and the compaction of the corresponding output sequence into a signature by the MISA has to be simulated for every fault of the fault model considered.

We now present a new method of constructing the cover circuit truth tables for a given CUT. Rather than using a deterministic construction, the new technique involves randomly choosing a specified percentage of the  $T$  cover

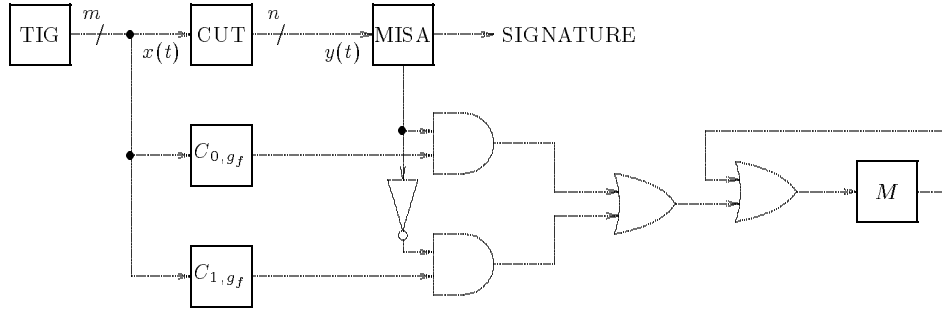


Fig. 2. Fault Detection Circuitry Combining BIST and Covers

circuit outputs to be active. Let  $100p$  be this percentage where  $0 < p < 1$ . Thus,  $p$  is the probability of a cover being active for a circuit output.

The truth tables for the cover circuits of a CUT are partially specified as follows. Let  $g$  be the function realized by the correct output of the MISA during the test. The input sequence to the cover circuits is the CUT input sequence  $x(0), \dots, x(T-1)$ . Partial specification of the cover circuits  $C_{0,g_f}$  and  $C_{1,g_f}$  for the CUT occurs as follows:

1. For each test input  $x(t)$ ,  $t = 0, \dots, T-1$ , check the value  $g_f(x(t))$ .
  - If  $g_f(x(t)) = 1$ , set  $C_{0,g_f}(x(t)) = 0$ .
  - If  $g_f(x(t)) = 0$ , set  $C_{1,g_f}(x(t)) = 0$ .
2. For each test input,  $x(t)$ ,  $t = 0, \dots, T-1$ , generate a random number  $v_t$  between 0 and 1. If  $v_t \leq p$ , mark the input.
3. For each marked entry  $x(t)$ , check to see which cover circuit output was set to 0 in Step 1.
  - If  $C_{0,g_f}(x(t)) = 0$ , set  $C_{1,g_f}(x(t)) = 1$ .
  - If  $C_{1,g_f}(x(t)) = 0$ , set  $C_{0,g_f}(x(t)) = 1$ .

The remaining unspecified values of the cover circuits are treated as don't-cares, and can be used to optimize the cover circuits. If an unspecified value of the covers is set to 1 for some input  $x(t)$ ,  $t \in \{0, 1, \dots, T-1\}$ , by the optimization, one of the covers becomes active for  $x(t)$  and the correctness of the corresponding output of the MISA is monitored. If the value is set to 0, both covers are inactive for  $x(t)$  and the corresponding output of the MISA is not monitored by the covers.

The number of inputs  $x(t)$ ,  $t \in \{0, 1, \dots, T-1\}$ , for which one of the covers is active cannot decrease by the optimization procedure. Thus, the relative frequency  $p'$  of one of the covers being active for  $x(t)$  after the optimization can be expected to be greater than  $p$  since some of the don't-care conditions are fixed to 1 during the optimization process.

#### IV. FAULT COVERAGE

We now evaluate the fault coverage of probabilistic cover circuits. Suppose that an arbitrary fault yields one of the  $2^r$  possible signatures with equal probability. With this assumption, the probability that an arbitrary fault results in the correct signature is  $2^{-r}$  [3]. Now consider a fault  $f_e$  which is mapped onto the correct signature of the MILFSR. Let the output sequence of the first stage of the MILFSR under this fault be denoted  $z_1(0) \dots z_1(T)$  with  $z_1(t) = z_1(t|f_e) \oplus \varphi(t)$  for  $0 \leq t \leq T$ ; thus,  $\varphi(t)$  is the error value in the first stage of the MILFSR. If  $\varphi(t) = 0$ , the first component of the state vector of the MILFSR is correct; if  $\varphi(t) = 1$ , this component is erroneous.

We assume that in the presence of an arbitrary fault in the CUT every sequence of states of length  $T$  of the MILFSR is equally likely. Then one has  $Pr(\varphi(t) = 1) = Pr(\varphi(t) = 0) = \frac{1}{2}$ . If the cover circuit is active for  $k$  inputs at times  $t_1, \dots, t_k$ , the fault will not be detected if  $\varphi(t_j) = 0$  for  $j = 1, \dots, k$ . This leads to the following lemma on fault coverage.

**Lemma.** *The probability of aliasing  $P_A$  for BIST combined with probabilistic cover circuits is given by*

$$P_A = 2^{-(r+k)}$$

where  $r$  is the number of stages in the shift register and  $k$  is the number of time steps at which the cover circuit is active.

**Proof:** For any  $t$ ,  $Pr(\varphi(t) = 1) = Pr(\varphi(t) = 0) = \frac{1}{2}$ . Hence, the probability that the fault  $f_e$  is not detected by the cover circuit is  $2^{-k}$ . The probability that an arbitrary fault will not be detected by signature comparison is  $2^{-r}$ ; thus, the overall probability of an arbitrary fault going undetected by the combination of BIST and cover circuits is  $2^{-(r+k)}$ .  $\square$

#### V. EXPERIMENTAL RESULTS

In this section we report the results of experiments conducted on several ISCAS'85 and Berkeley benchmark circuits. The simulations not only confirm the theoretically

predicted improvements of the aliasing probability, but show that the improvement is significantly better than predicted. Moreover, the hardware cost is nearly always negligible compared to the size of the CUT. For example, for C880 an aliasing probability of approximately  $2^{-166}$  is achieved with tests of length 1000 using only 19 additional gates. An additional 140 stages would have to be added to the MISA to obtain this aliasing probability with no cover circuit.

The simulation experiments were conducted using the Lg3 functional fault simulator written by R. Byrne [11] at the University of Victoria. The simulator assumes the single stuck-at fault model with fault collapsing. The simulator performed the functional fault simulation and the CUT output sequence compression. Each simulation produced a fault-free sequence of states for the MISA under the given test sequence.

Table I shows the statistics of the circuits used in the simulation experiments. C432, C499, C880, C1355, C1908, and C3540 are ISCAS'85 benchmark circuits. IN5, IN7, X1DN, X9DN, and VG2 are Berkeley circuits [12].

Initially, complete test simulation experiments were performed on the circuits in Table I. VG2, X1DN, and X9DN were omitted due to the extreme length of their tests. The test sequences for the ISCAS'85 benchmark circuits were deterministic tests generated by the ATLANTA test pattern generation program [13]. The test sequences for the Berkeley benchmark circuits were pseudo-random sequences generated using the method presented in [12]. We received appropriate feedback polynomials and initial states for the Berkeley circuits from the authors of [12].

Twenty constructions were performed for each circuit and each value of  $p$ . Experimental constructions were performed with all circuits for  $p = 0.40, 0.25$ , and  $0.10$ . Experiments with  $p = 0.75$  were then run for the short-test ISCAS'85 circuits, while  $p = 0.01$  experiments were conducted on the long-test circuits IN5 and IN7. A detailed report of these experiments can be found in [14].

The complete test ISCAS'85 simulations yielded very good results. For  $p = 0.75$ , the total cover size ranged from 7.14% of the CUT for C432 (14 gates) to 1.86% for C3540 (32 gates). The corresponding aliasing probabilities for the ISCAS'85 circuits ranged from  $2^{-47}$  to  $2^{-148}$ . Between 40 and 126 stages would have to be added to the MISA to obtain a similar  $P_A$  without covers.

The overhead for the covers constructed for IN5 and IN7 was much higher than for the ISCAS'85 circuits; for  $p = 0.40$ , best covers for IN5 were 262.50% of the CUT and for IN7 were 33.33% of the CUT. The corresponding test sequences were, however, significantly longer, and the increased test length provided a dramatic reduction in  $P_A$ . For  $p = 0.40$  with the best covers, the IN5 probability of aliasing was  $2^{-3715}$  and for IN7  $P_A$  was  $2^{-9231}$  (essentially zero). In other words, far smaller values of  $p$  would suffice to achieve a comparable probability of aliasing. For

example, when  $p = 0.01$ , best covers for IN5 were only 22.92% of the CUT, and for IN7 were only 9.40%, with corresponding aliasing probabilities of  $2^{-152}$  and  $2^{-8860}$ , respectively.

To obtain a baseline set of cover circuit sizes for the circuits in Table I, a test length of 1000 was chosen, and tests for  $p = 0.25$  and  $p = 0.10$  were run for each circuit. For the Berkeley circuits, the test sequences were generated by taking the first 1000 test vectors in the complete test as specified in [12]. For the ISCAS'85 circuits, the tests were generated by linear feedback shift registers. Ten simulated constructions were performed for each circuit and each value of  $p$ .

Table II shows the best and average results of the simulations for  $T = 1000$ . The *Circuit* column gives the name of the circuit, while the column labeled  $p$  reports the value of  $p$  for the corresponding experimental results. The *Best Covers* column reports the total overhead for the smallest zero cover and one cover constructed for the given value of  $p$ . The overhead is reported as a percentage of the size of the corresponding CUT, and two values for the overhead are reported. The first is the overhead of the best covers assuming that inverted values for all input lines are available, and the second value includes the cost of inverting the required input lines. The column  $p'$  reports the proportion of cover circuit outputs active after the optimization process. In the  $P_A$  column, the probability of aliasing is given assuming the use of the best covers. The *MISA Stages* column gives the number of stages which would have to be added to the MISA to achieve the aliasing probability achieved with the best covers. The average cover sizes for the simulations are reported in the *Average Covers* column, in the same format as the *Best Covers* column. The final column in the table, *Standard Deviation*, reports the standard deviation of the cover sizes (as a percentage of the CUT) for each set of simulations.

The data in Table II show many interesting properties of the construction process. Circuits with a similar number of gates had cover circuits of very similar sizes. For the circuits of approximately 200 gates, the covers required just over 40% of the size of the CUT including line inversion costs for  $p = 0.25$ . When  $p$  was reduced to  $p = 0.10$ , however, the size of the covers was reduced to about 25% of the size of the CUT while a significant reduction in  $P_A$  was still obtained.

The fixed test length simulation experiments also showed that as the size of the circuits increased for fixed  $T$ , the cover circuit percentages decreased significantly. For example, C432 (196 gates) with  $p = 0.25$  required 41.84% of the CUT overhead, while C3540 (1719 gates) required only 4.71%. In fact, the simulations for test length 1000 and  $p = 0.25$  yielded best covers (including inversion costs) of between 76 and 85 gates for circuits which ranged between 189 and 1719 gates. Thus, the size of the covers seems to remain fairly constant for fixed test length, independent of the size of the CUT.

TABLE I  
CIRCUITS USED IN SIMULATION.

| Circuit Name | Number of Inputs | Number of Outputs | Gates | Faults in LG3 Fault Model | Test Length |
|--------------|------------------|-------------------|-------|---------------------------|-------------|
| C432         | 36               | 7                 | 196   | 507                       | 50          |
| C499         | 41               | 32                | 243   | 750                       | 54          |
| C880         | 60               | 26                | 443   | 942                       | 54          |
| C1355        | 41               | 32                | 587   | 1566                      | 85          |
| C1908        | 33               | 25                | 913   | 1870                      | 121         |
| C3540        | 50               | 22                | 1719  | 3120                      | 155         |
| IN5          | 24               | 14                | 192   | 630                       | 6530        |
| IN7          | 26               | 10                | 117   | 331                       | 9274        |
| VG2          | 25               | 8                 | 189   | 581                       | 111456      |
| X1DN         | 27               | 6                 | 207   | 618                       | 838176      |
| X9DN         | 27               | 7                 | 215   | 643                       | 446624      |

IN7 is an exception to the above observation; the best covers for test length 1000 and  $p = 0.25$  required only 16 gates. IN7, however, shows that there are some specific circuits which are extremely amenable to the optimization process. Even for very low values of  $p$ , IN7 always had  $p'$  over 0.90. This implies that  $p$  can be chosen to be very small to yield small covers, while a large reduction in probability of aliasing will still be achieved because  $p'$  will be very high.

The very small standard deviation of the size of the cover circuits shows that the construction method provides very consistent results. This fact also suggests another approach for selecting the best simulation result. Rather than taking the result with the smallest number of gates, the best experiment could be chosen to be the one which gives the lowest probability of aliasing, with only a small increase in overhead over the smallest construction. For example, consider C3540. The best covers for  $p = 0.75$  required 81 gates, or 4.71% of the CUT, with a probability of aliasing of  $2^{-378}$ . The run which yielded the lowest probability of aliasing,  $2^{-403}$  required 87 gates or 5.06% of the CUT. Thus, for the extra overhead of 6 gates or 0.35% of the CUT, the probability of aliasing can be reduced by a factor of  $2^{-25}$ .

In the simulations for  $T = 1000$ , no aliased fault went undetected by the covers. This fact is very important. The simulations show that for circuits with larger test lengths, even a small value of  $p$  will allow a very high percentage of aliased faults to be detected. This agrees with the theoretical analysis which showed a significant reduction in the probability of aliasing for small values of  $p$ .

## VI. CONCLUDING REMARKS

We presented a circuit-independent method of reducing aliasing in built-in self-test. Cover circuits are constructed with randomly chosen active outputs based on a given

probability  $p$ . An expression for the probability of an erroneous output sequence going remaining undetected is derived. The aliasing probability is shown to decrease exponentially fast with increasing test lengths.

Simulation results are presented for both ISCAS'85 and Berkeley benchmark circuits. The simulations corroborate the theoretically predicted properties. Adding a randomly chosen cover circuit to a standard BIST circuit will lead to a significant decrease of the aliasing probability. To achieve such an improvement, only very little additional hardware is required. Moreover, very short test input sequences suffice to obtain this high degree of fault coverage.

In summary, the simulation results indicate that the method presented permits an enormous improvement of the aliasing probability in a far more economical way than by increasing the size of the MISA or by ODM [1]. Moreover, the parameter  $p$  allows control of the tradeoff between the size of the cover circuits and the reduction in aliasing probability. Without modification, our method can also be applied together with the multiple-signature analysis of [4] and [5], reducing the aliasing probability even further.

The results presented in this paper do not take into consideration faults in the cover circuits. In [3], however, a method is given for detecting faults in the cover circuits as well as the CUT. Future research possibilities include verification of the feasibility of the method on larger circuits, and implementation of built-in self-test with the self-checking cover circuit.

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TABLE II  
BEST AND AVERAGE COVERS FOR T=1000 SIMULATIONS.

| Circuit | $p$  | Best Covers<br>(% of CUT) | $p'$ | $P_A$      | MISA<br>Stages | Average Covers<br>(% of CUT) | Standard<br>Deviation |
|---------|------|---------------------------|------|------------|----------------|------------------------------|-----------------------|
| C432    | 0.25 | 23.47 (41.84)             | 0.34 | $2^{-351}$ | 344            | 25.36 (43.67)                | 1.02 (1.12)           |
|         | 0.10 | 12.76 (24.49)             | 0.17 | $2^{-174}$ | 167            | 13.62 (26.17)                | 0.46 (0.86)           |
| C499    | 0.25 | 18.11 (34.98)             | 0.34 | $2^{-368}$ | 336            | 19.42 (35.84)                | 0.88 (1.05)           |
|         | 0.10 | 8.23 (15.64)              | 0.14 | $2^{-173}$ | 141            | 10.08 (19.18)                | 0.89 (1.70)           |
| C880    | 0.25 | 9.03 (17.16)              | 0.35 | $2^{-379}$ | 353            | 9.66 (18.67)                 | 0.49 (1.09)           |
|         | 0.10 | 4.29 (8.13)               | 0.14 | $2^{-166}$ | 140            | 5.01 (9.50)                  | 0.33 (0.65)           |
| C1355   | 0.25 | 7.50 (14.31)              | 0.33 | $2^{-363}$ | 331            | 8.25 (15.16)                 | 0.40 (0.40)           |
|         | 0.10 | 3.58 (6.81)               | 0.15 | $2^{-185}$ | 153            | 4.34 (8.30)                  | 0.34 (0.69)           |
| C1908   | 0.25 | 5.26 (8.87)               | 0.36 | $2^{-387}$ | 362            | 5.72 (9.31)                  | 0.34 (0.34)           |
|         | 0.10 | 2.41 (4.60)               | 0.13 | $2^{-157}$ | 132            | 2.90 (5.52)                  | 0.27 (0.54)           |
| C3540   | 0.25 | 2.44 (4.71)               | 0.36 | $2^{-378}$ | 356            | 2.58 (4.97)                  | 0.09 (0.17)           |
|         | 0.10 | 1.16 (2.21)               | 0.15 | $2^{-171}$ | 149            | 1.33 (2.51)                  | 0.12 (0.25)           |
| IN5     | 0.25 | 29.17 (41.67)             | 0.35 | $2^{-363}$ | 349            | 31.61 (44.11)                | 1.36 (1.36)           |
|         | 0.10 | 14.06 (26.56)             | 0.16 | $2^{-178}$ | 164            | 15.78 (28.07)                | 1.14 (1.20)           |
| IN7     | 0.25 | 7.69 (13.68)              | 0.96 | $2^{-968}$ | 958            | 9.06 (15.64)                 | 0.68 (1.43)           |
|         | 0.10 | 5.98 (10.26)              | 0.91 | $2^{-920}$ | 910            | 7.01 (11.54)                 | 0.51 (1.03)           |
| VG2     | 0.25 | 29.63 (42.86)             | 0.35 | $2^{-355}$ | 347            | 30.85 (44.07)                | 0.75 (0.75)           |
|         | 0.10 | 14.81 (28.04)             | 0.17 | $2^{-174}$ | 166            | 16.35 (29.37)                | 1.26 (1.36)           |
| X1DN    | 0.25 | 25.60 (38.65)             | 0.40 | $2^{-405}$ | 399            | 26.86 (39.90)                | 0.84 (0.84)           |
|         | 0.10 | 12.56 (23.67)             | 0.18 | $2^{-181}$ | 175            | 14.44 (27.00)                | 0.88 (1.30)           |
| X9DN    | 0.25 | 25.58 (38.14)             | 0.38 | $2^{-391}$ | 384            | 26.60 (39.16)                | 1.10 (1.10)           |
|         | 0.10 | 11.63 (22.79)             | 0.15 | $2^{-153}$ | 146            | 13.44 (25.81)                | 0.96 (1.02)           |

R. Byrne for the use of the LG3 fault simulator.

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