System-level Verification of CDMA Modem ASIC

GyeongLyong Park, KyungHi Chang, Jaeseok Kim, and Kyungsoo Kim

VLSI Architecture Section
Electronics and Telecommunications Research Institute
Yusung P.O. Box 106, Taejon, 305-600 Korea
Tel: +82-42-860-6226
Fax: +82-42-860-6200
Email: jskim@cadvax.etri.re.kr

Abstract - In this paper, we present a system-level verification methodology which is used to verify the design of CDMA (Code Division Multiple Access) modem ASIC. To make the system-level verification feasible, the models for modulator of base station, fading channel and AGC loop were developed under the C environment. Behavioral modeling of a microcontroller was also carried out using VHDL to provide the ASIC with realistic input data, and the netlist of CDMA modem ASIC is loaded on to a hardware accelerator, which is interfaced with VHDL simulator. Finally, simulation was performed by executing an actual CDMA call processing software. This method was proved to be effective in both discovering in advance malfunctions of ASIC when embedded in the system and reducing simulation time by a factor of as much as 20 in the case of gate-level simulation. The designed ASIC which consists of 90,000 gates and 29K SRAMs is now successfully working in the real mobile-station on its first fab-out.

I. INTRODUCTION

Communication systems have been usually simulated under the environment of the high-level language such as C. However, employing that approach makes behavioral simulation and implementation as separate efforts. A better alternative may be the use of VHDL [1]. Developing VHDL behavioral models at the early stage of system design offers many advantages. First of all, the same stimuli can be applied to the simulation of both system algorithm and logic design. This makes it easier to confirm correct implementation of the algorithm.

In addition, the behavior of the ASICs as well as proper interface among them can be tested by executing an actual application software. This kind of system-level verification is an invaluable technique, because there exist difficulties in generating all the necessary test vectors to confirm the functionality of each ASICs.

The only downside of this method is the increasing simulation time as the size of ASICs is increased. The effectiveness of this simulation method can be enhanced further, however, by setting up an environment where some of the components of the system under test are replaced with actual hardware, and interfaced with Hardware (H/W) Modeler [2]. At the same time, H/W Accelerator (e.g. IKOS NSIM64 [3]) can be used in parallel with H/W Modeler.

In this paper, we present a methodology and CAD environment which is used for pre-silicon system-level verification of ASIC chip-sets in VHDL system model. Followed by a brief overview of CDMA system [4], We describe the environment which consists of base station modulator model, fading channel & AGC(automatic gain control) loop model, and microcontroller VHDL model. Finally, one of the verification results with a successful development of modem ASIC is presented.

II. OVERVIEW OF CDMA MOBILE STATION

Digital cellular communications are increasingly replacing analog counterparts because they offer big improvements in channel capacity, noise immunity, and low

cost. Code division multiple access(CDMA) is one of the digital cellular systems which is replacing the analog cellular systems. CDMA MS(mobile station) shown in Fig. 1 is composed of RF system, IF system, analog baseband system, and digital baseband system. Key components of digital baseband system are modem ASIC, digital signal processor (DSP) which performs variable rate vocoding algorithm, 16-bit microcontroller, and operating software coded in 512 Kbyte ROM. Modem ASIC which performs modulation and demodulation of wideband spread spectrum signal, is composed of modulator, demodulator and Viterbi decoder. Modulator includes the function of r=1/3, K=9 convolutional encoding, block interleaving which spans 20msec frame, 64-ary orthogonal modulation, OQPSK spreading, FIR filtering, and deinterleaving. Demodulator contains searcher, fingers and combiner to perform demodulation of wideband spread spectrum signals. Searcher detects pilot channel, and fingers do short PN despreading, orthogonal demodulation, timing deskew, pilot energy measurement, frequency error signal generation and timing tracking. Combiner takes roles of combining finger outputs, extraction of power control bit, long PN despreading and reference clock generation. Demodulator extensively interacts with CPU, and its performance is very closely related to the CPU software. Viterbi decoder is used to near optimally decode synchronized and quantized symbol stream from the deinterleaver block of the modulator.

III. SYSTEM VERIFICATION ENVIRONMENT

The top-down ASIC design starts with an ASIC requirement specification, followed by a behavioral verification of system/ASIC algorithms. However, analyzing the behavior of ASIC may not be sufficient to detect all the errors in the circuit. In such cases, RTL or gate-level description is more appropriate for pin-pointing the errors related to the critical behavior of the ASIC. Considering above all possibilities makes mixed-level simulation with VHDL simulator as the best candidate for the overall system simulation.

Our system-level verification method focuses on the modeling of the target system rather than ASIC components. The true testing of the working target system is accomplished by running its application software thereby checking its actual function in real situation. Even though it still has some limitations, this kind of logic emulation may be a key technology for verifying the system performance before implementation and for system-level HW/SW debugging. For this purpose, we prepared VHDL models of CPU and memory to run the actual application software, and rake receiver input patterns generated using signal processing workstation(SPW) [5]. Overall verification environment for CDMA MS system which consists of base station modulator model, fading channel & AGC loop model, microcontroller VHDL model, and a simplified version of operation software is shown in Fig. 2.

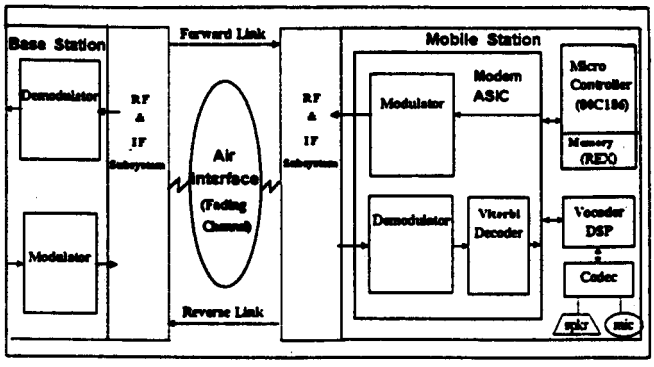

Fig. 1. Structure of CDMA Mobile Station

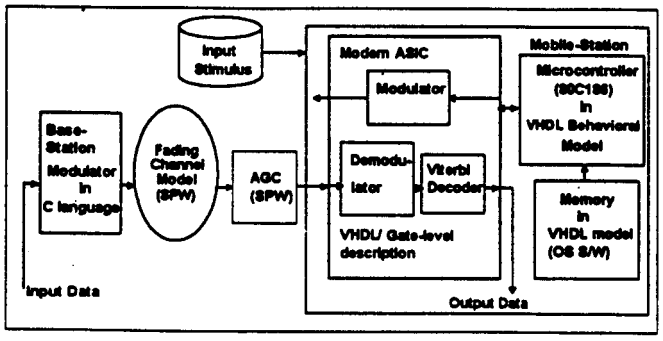

Fig. 2. Verification environment for CDMA Mobile Station

A. Base Station Modulator Model

Base Station modulator of CDMA system has been modeled using SPW to produce input stimulus for CDMA MS modem ASIC by the requirement of IS-95 [4]. Fig. 3 shows this model. At first, frame data is channel coded by appending CRC, convolutional encoding and interleaving for pilot, sync, paging and traffic channels. These symbols further go through long-code scrambling (only for traffic channel), power control bit insertion (only for traffic channel), Walsh modulation and I and Q-channel PN spreading. The blocks in Fig. 3 is linked with C program by using C-language interface utility 'Custom Coded Block' supported by SPW, and they are directly accessible by the simulator.

B. Fading Channel and AGC Loop Model

To perform the requirement proposed by IS-95, two kinds of channel model is necessary. One is AWGN (Additive White Gaussian Noise) model, and the other is fading channel model. The AWGN model which has an effect only by the received E_b/N_0 always performs better than the fading model, and that model is proud of its simplicity. The wideband fading channel model with Rayleigh fader, which is our concern, described by TR 45.5.3.1 has following characteristics [6].

- 3-ray Rayleigh fading model
- Independent fading statistics for each path
- Same average power for all 3 paths
- Constant delay of 1.5us and 14.5us for the 2nd and 3rd paths respectively from the first path
- 3 vehicle speeds: 8, 50, and 100 km/h

A ray of the described 3-ray fading channel is modeled as shown in Fig. 4, where P=1/6.

The output of above channel model is applied to the AGC loop for the purpose of compensating the attenuated signal power due to multipath fading channel. AGC loop not only keeps the constant received signal power, but controls transmit power. Fig. 5 shows an AGC loop model which consists of a received signal strength indicator (RSSI) path and a RSSI reference value (REF) path.

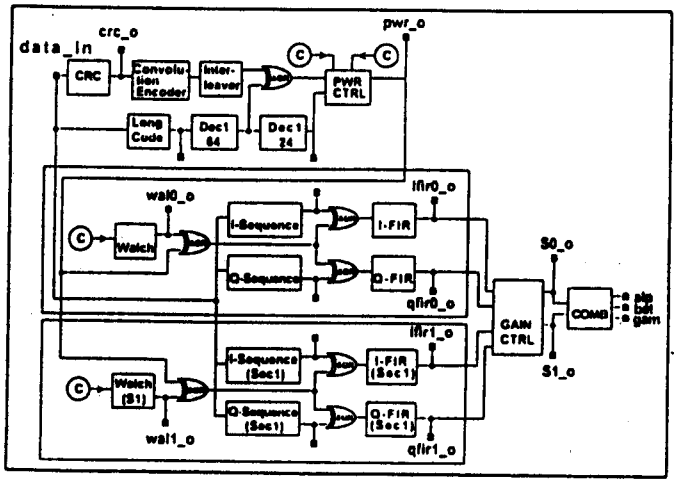

Fig. 3. Model of CDMA base station modulator

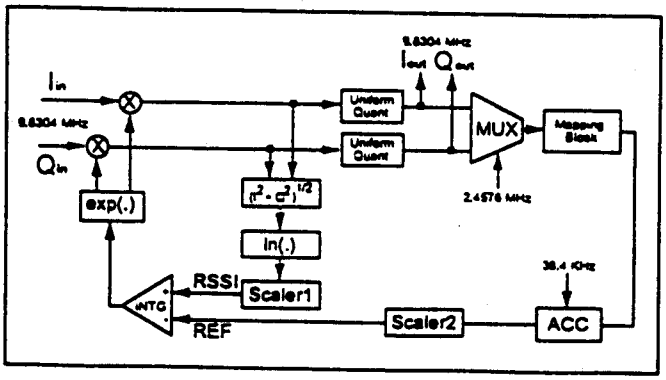

Fig. 4. A single ray of the multipath fading channel model

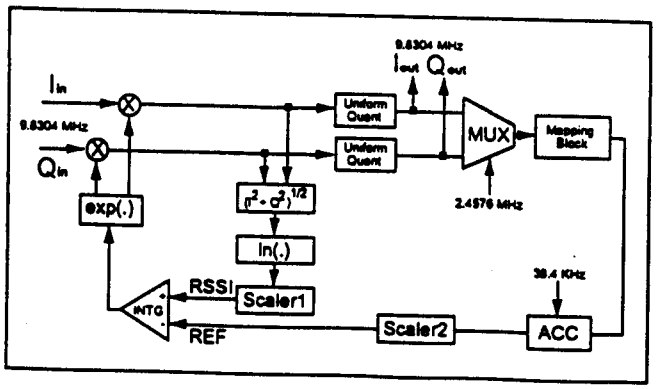

Fig. 5. Model of AGC loop

RSSI path behaves as a compander on the magnitude of quadrature signal, and the components of REF path are uniform quantizer, multiplexer, mapping block and accumulator. Scaler1 and Scaler2 blocks are added to match the signal level of each path. To guarantee the 80 dB of dynamic range at least, AGC supports upto 10^4 of gain control. Then, AGC loop forces the error between RSSI and REF to zero. The retrieved signal is 4-bit quantized and applied to the demodulator of MS modem ASIC.

C. Microcontroller VHDL Model

A VHDL behavioral model of 16-bit microcontroller has been developed because our main purpose was verifying the functionality of ASICs under development rather than designing a microcontroller. By using higher abstraction levels, simulation time can be greatly reduced. The microcontroller we modeled is shown in Fig. 6 and it is functionally compatible with Intel 80C186 microcontroller [7]. The behavioral model of this microcontroller consists of seven separate entities in VHDL. Each of these entities except for the watchdog timer corresponds to the functional block of 80C186. However, our microcontroller model differs from the 80C186 in several aspects. First of all, the required features for interfacing the microcontroller with a coprocessor were not implemented. Furthermore, it does not include the DRAM refresh unit.

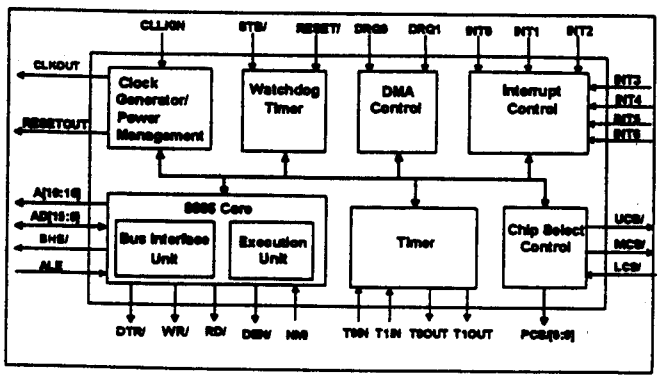

Fig. 6. Block diagram of 16-bit microcontroller model

Among the three independent timers within the timer unit, only one timer is allowed to operate in the alternating mode. Instead of providing five chip enable signals for memory, the model generates only one mid-range chip select (MCS), thus the total chip enable signals for memory being three. As a consequence, the size of the memory enabled by each chip select pin was modified. Unlike the interrupt controller in 80C186, the interrupt controller in the microcontroller does not support the slave mode. It rather operates only in the fully nested mode as a master. In addition, it provides seven external pins to accept interrupt requests. Finally, the watchdog timer unit is included for supervising the system of interest. The other two functional blocks, namely the clock generator and the DMA controller, are compatible with those in 80C186.

The functionality of the microcontroller model was verified by first running an assembly program and investigating the results. For this purpose, we used the bootstrap program of the application software developed for the system of interest. We then prepared test programs in C language to confirm the proper behavior of each peripherals. For example, we had to develop a program to verify if multiple interrupt requests are correctly nested. Finally, we executed the application software written in C language and compared the results with those obtained by running the same program with the actual 80C186 installed in an in-circuit emulator. The behavioral model consists of about 11,000 executable lines, and it takes about 40 second with QUICKVHDL of Mentor Graphics to simulate the microcontroller for 1 ms of real time.

D. Application Software as a Testbench

A simplified version of the actual application software was used as a stimulus to simulate main functions of CDMA modem ASIC. The software for the mobile station provides overall control for functions by the CDMA modem ASIC.

Upon startup, the software first performs an initialization of CDMA modem ASIC. Following the initialization, it performs the pilot channel acquisition, parsing the received sync channel message, system time change . (long-code assignment), parsing the received paging channel data and forward traffic channel data, access attempt procedure on access channel, and the transmission of preamble and null traffic data on the reverse traffic channel.

The mobile station software was first compiled to generate object files. These files were linked and located to produce an Intel Hex format, from which we could get the physical address for each machine codes to be downloaded to the memory VHDL model. The VHDL model of 16-bit microcontroller can execute the main control processing by accessing the program downloaded to memory model.

IV. VERIFICATION PROCESS AND RESULTS FOR CDMA MODEM ASIC

With the above modeling, system-level verification of CDMA MS modem ASIC is performed by executing the actual application software. CDMA modem ASIC which is designed by RTL-level VHDL is interfaced with real CPU chip on H/W Modeler. To reduce the simulation time of RTL-level ASIC, H/W accelerator is exhaustively used. Under these whole simulation environment of mixed-level, satisfactory operation of MS was observed.

Associated with performing system simulation, several factors should be taken into consideration such as simulation time required and securing simulation library of the cells used in the RTL models. Owing to the large scale of the system of interest, simulation of the whole system in software environment seemed infeasible in terms of simulation time. We, therefore, connected the microcontroller with one functional module in MS at a time and simulated the subsystems thus formed. In an effort to emulate the effects of the whole system simulation as much as possible under the given circumstances, we carefully investigated the simulation results from each subsystems to prepare the input stimuli for other subsystems. That is, in case a signal is generated by one module and passed as an input signal to another functional block, timing information of the signal obtained during simulation of the former was used to prepare the input stimulus for simulation of the latter.

To simulate the system by executing the actual application software, the program was first compiled to generate object files. These files were linked and located to produce a hex file of Intel format, from which we could get the physical address for each machine codes to be downloaded to the memory VHDL model. At the same time, channel modeling [6], which includes the fading effects, was also carried out using SPW to provide input signals for both I and Q channels of the demodulator. During system simulation, emphasis was placed on verifying the proper communication between the microcontroller and other modules, since the functionality of each modules was previously confirmed even though the confirmation was rather tentative.

Fig. 7 shows an example of simulation results. It shows the process where the searcher is reporting measured energy to the microcontroller by DMA for pilot acquisition, accomplishing the slew at the slew command by the microcontroller.

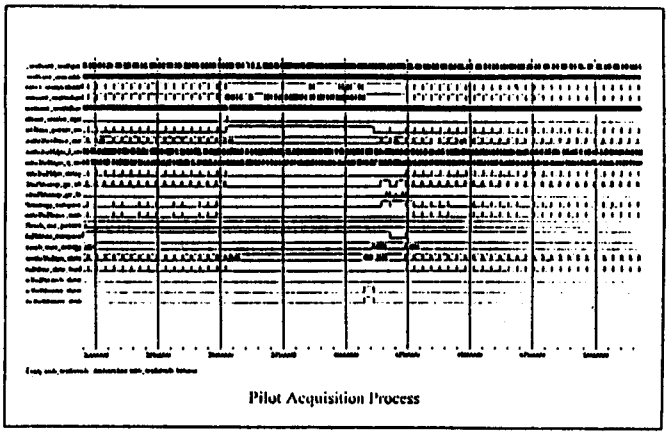

Fig. 7. An example of simulation results

We could identify a number of errors in the RTL description of the functional modules while performing system simulation. Most of these mistakes stem from lack of good understanding on the proper interface between the microcontroller and the modules as well as among the functional blocks themselves. One of the most critical problems was that some of the modules could not be initialized properly by the microcontroller. There were three causes for this difficulty, one of which was that timing between the microcontroller and the modules did not have enough margin. Another reason was that the initialization sequence depicted in the application software is not compatible with the RTL description. The other cause was that some of the input signals to a given module are not driven in time by other modules resulting in failure of the system initialization. After all the necessary corrections, the system was successfully initialized and commenced its proper operation.

When we used an usual simulator to simulate the MS system for 40 ms of real time which is a half of superframe, it took about 30 hours on SPARC20 workstation and we could not go further due to the limitation of workstation capacity. By using the H/W accelerator connected to the VHDL simulator, we could simulate 7 superframes (560 msec in real time) within 27 hours which is almost minimally necessary to confirm the call processing of CDMA system.

V. CONCLUSIONS

System-level verification methodology used for developing CDMA modem ASIC was presented in this paper. To carry out the system-level simulation, models of the base station modulator, the fading channel, the AGC loop, and the microcontroller were developed and interfaced with a RTL description of the modem ASIC. As much as possible, we tried to model the real hardware accurately so that the output of the above models can be directly utilized to verify the system-level operation of CDMA modem ASIC. It was found that some of the errors in the RTL description of the ASIC were overlooked during stand-alone simulation of each modules. Successful operation of MS system was observed after all the corrections had been made. The modem ASIC which consists of 90,000 gates and 29K SRAMs is now successfully working in the real CDMA Mobile Station on its first fab-out.

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