Integrated interconnect circuit modeling for VLSI design

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Abstract - An integrated interconnect modeling system, SIMS, is developed with the parametrized modeling of interconnect and the interface with a schematic capture and editor. SIMS automatically drives numerical interconnect simualtion as directed by technology engineers, creates polynomial model library for interconnect parasitics, generates netlist including SPICE model for the interconnect structure specified by circuit designers, automatically drives circuit simulations and display the simulation results through advanced GUI.. VLSI design with SIMS makes it possible to consider parasitic effects fast and accurately, which becomes more important in deep submicron circuit design area. With this capability, circuit design with optimized interconnect layout can be easily achieved. Ultimately the integrated system helps to reduce the cost of technology development and the time-to-market by building up the concept of design-for-manufacturability.

1. INTRODUCTION

As chip density and circuit switching speed are improved, the parasitic effects induced by the interconnect has emerged as one of the most critical factors in restricting circuit performances.[1] In order to ensure in-spec design, the parasitic effects should be taken into account as accurately and as early in design flow as possible.

There have been several approaches to accomplish this. Earlier, simplified analytical models were used to estimate interconnect capacitances, which could not meet the level of accuracy required by the present VLSI technology.[2] With the advent of numerical interconnect simulator, another approach based on simulation and extraction of interconnect capacitance was proposed to overcome this difficulty.[3]

However, an accurate interconnect modeling system which aims at the enhancement of design efficiency should be integrated with the existing design methodology. It is the purpose of this work to provide such an integrated design environment, called SIMS(SPICE Interconnect Modeling System), to the design community.

In this paper, the general concept and the structure of the system SIMS and the capacitance modeling which makes the embodiment of the system possilbe will be presented.

2. SYSTEM OVERVIEW

The conceptual diagram of the system structure is shown in Fig 1. SIMS is composed of two separate modules, called SIMG and ESCAPE respectively.[4] SIMG automatically drives 2D/3D numerical interconnect simulator according to the interconnect structure descriptions input by the technology engineers and generates interconnect model library. ESCAPE is the in-house schematic capture tool which, as directed by the types of interconnect specified by a designer, accesses the interconnect model library generated by SIMG, creates the netlist including interconnect capacitances, drives circuit simulations and provides real-time verification of the circuit functionality affected by interconnect through advanced GUI.

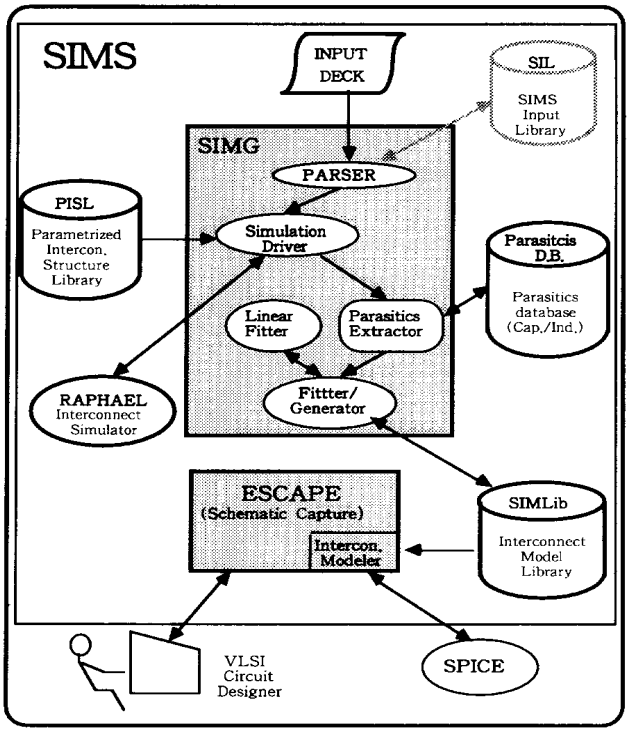


Fig.1 The concept of SIMS(SPICE Interconnect Modeling System)

3. SIMG(SPICE Interconnect Model Generator)

As seen in Fig.1, SIMG consists of 4 submodules of PARSER, simulation driver, parasitics extractor and fitter/generator. Parser takes the input deck, reads in data from SIL to create the simulation input and structure, and sends this information to simulation driver. Then, the simulation driver initiates numerical interconnect simulations to calculate the parasitics as functions of layout parameters. The parasitic extractor extracts the parasitics from the simulation results and stores them into the parasitic database. Finally, the fitter/generator creates interconnect model library based on least square fit. The automatic real-time verification is implemented to examine the accuracy of the model for arbitrary design parameters.

SIMG creates data library for simulation inputs and interconnect structures for the ease of use and library management as technology changes . Not only the layout parameters like interconnect line width, length and spacing but also the technology parameters such as material constants, layer thicknesses and resistivities can be assigned in the input file. Also the hierarchy and the objectivity of the input data allow the model library manager to maintain structured database. The system environment can be set either by UNIX shell variables or by setup files for improved maintenance of the system.

4.PARAMETRIZATION OF THE INTER CONNECT STRUCTURE

SIMG performs the numerical simulations varying the layout parameters after it reads in the parametrized interconnect structure template file. The parametrization of the interconnect structure is performed by the simulator's keyword ".param" as following ;

.param parameter name1 = parameter value1;
.param parameter name2 = parameter value2;
:

SIMS searches for the name of the parameter declared in the input deck among interconnect template structure files, and transforms the value of the parameter. The structure file translated as such is fed into the simulator as an input file for simulation.

5. PARASITICS DATABASE

To generate models for an interconnect structure, tens or hundreds of numerical simulations have to be performed each of which could take several minutes. Therefore, when an unexpected accident takes place or when model options have to be changed during simulation, a large amount of time will be required for redoing simulations.

SIMS has the built-in parasitics database for storing and fetching out the parasitic values for the same layout and/or technology parameter values in the simulation.

6. INTERCONNECT CAPACITANCE MODELING

A. Parametrization of parasitic capacitance

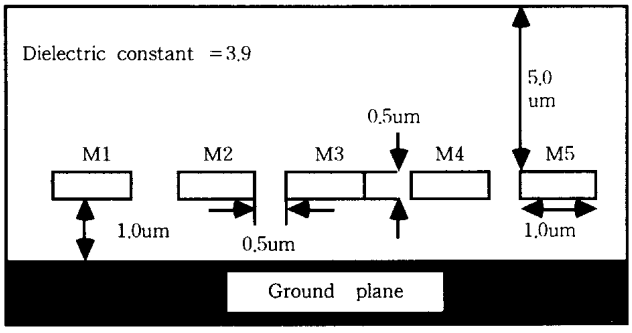
The interconnects used in IC chips can be approximately described as the array of interconnects which are placed parallel to each other above the ground plane as shown in Fig. 2. The capacitance of each interconnect in this array is represented by the sum of all capacitances with other interconnects as well as that with the ground plane. However as the simulated capacitance matrix shows in Fig.2, the contribution in capacitance from other interconnects is orders of magnitude smaller than that from the two nearest-neighbor interconnects, and hence can be neglected.

From this observation, the capacitance of each interconnect can be given by:

$$C_{inner} = C_g + 2*C_i \quad (1.1)$$
$$C_{edge} = C_g + C_i \quad (1.2)$$

where C_{inner} and C_{edge} are the capacitances of interconnect placed inside and at the edge of the array respectively, and C_g and C_i are the capacitances of each interconnect with the ground plane(called ground capacitance) and with one of its nearest neighbors(called coupling capacitance), respectively.

The parameters which affect interconnect capacitances can be grouped into the technology parameters and layout parameters. Technology parameters such as layer thicknesses and resistivities, dielectric constant can be considered fixed and cannot be changed for optimization by designers once



	M1	M2	M3	M4	M5
M1	4.9E-16	2.3E-16	4.6E-18	1.7E-18	1.2E-18
M2	2.3E-16	4.9E-16	2.3E-16	4.6E-18	1.7E-18
M3	4.6E-18	2.3E-16	4.9E-16	2.3E-16	4.6E-18
M4	1.7E-18	4.6E-18	2.3E-16	4.9E-16	2.3E-16
M5	1.1E-18	1.7E-18	4.6E-18	2.3E-16	4.9E-16

Fig.2 The result of simulation of coupling capacitance between wire and other wire when five parallel metal strip lines run groundplane

the technology process specifications are defined. On the other hand, layout parameters are flexible to be optimized for performance.

Therefore in a given process, the interconnect capacitance can be described as a function of layout parameters.

C=f(layout parameters, tech. parameters=const.) (2.1)
C=f(layout parameters)
when technology parameters are fixed (2.2)

From the analysis of simulation results for interconnect capacitance, it is found that the interconnect capacitance is linearly proportional to the line length, and to the line width provided that the width is not too small. A strong nonlinearity in the dependence on width shows up for small width and also on spacing for all the range of line spacing.

From the above results, the interconnect capacitance can be expressed as a function of layout parameters as follows:

$$C(L,S,W) = L*C_{s,w}(S,W) \quad (3)$$
$$C_{s,w}(S,W) = C_{w0}(S) + F_s(W)\{C_{w1}(S) - C_{w0}(S)\} \quad (4)$$

where $C_{w0}(S)$ and $C_{w1}(S)$ are the capacitances per unit length at the minimum width of W_0 and at the maximum width of W1 in the width range, respectively. $F_s(W)$ becomes $(W-W_0)/(W_1-W_0)$ for $W_c<W_0<W<W_1$ where W_c is the critical width below which the non-linearity shows up.

In case the capacitance is not linearly proportional to the interconnect width, the capacitances for $S=S_1$, $S=S_2$, $S=S_3$,...., and $S=S_i$ in a given range(S_{min},S_{max}) can be expressed as follows:

$$C_{s=s1,w}(W) = C_{w0}(S1) + F_{s1}(W)*\{C_{w1}(S_1) - C_{w0}(S_1)\} \quad (6.1)$$
$$C_{s=s2,w}(W) = C_{w0}(S2) + F_{s1}(W)*\{C_{w1}(S_2) - C_{w0}(S_2)\} \quad (6.2)$$
$$C_{s=s3,w}(W) = C_{w0}(S3) + F_{s1}(W)*\{C_{w1}(S_3) - C_{w0}(S_3)\} \quad (6.3)$$
$$\vdots$$
$$C_{s=si,w}(W) = C_{w0}(Si) + F_{s1}(W)*\{C_{w1}(S_i) - C_{w0}(S_i)\} \quad (6.4)$$

In this case, Fsi(W) are nonlinear functions of W whose value ranges from 0 to 1. It is shown in Fig. 3,4 that Fs1(W), Fs2(W), ... , and Fsi(W) can be represented by the generalized function, Fs(W).

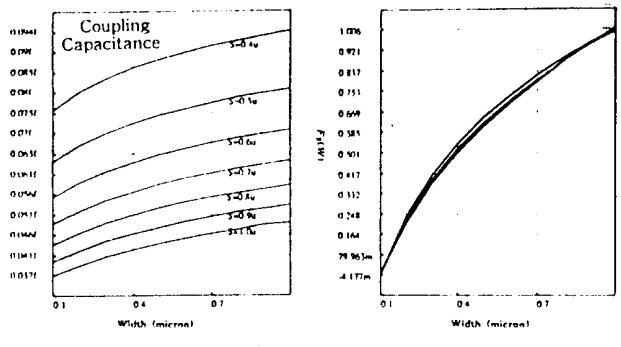
In SIMS, Cw(S) and Fs(W) are represented by the n-th order polynomial as following:

$$C_w(S) = \sum_{i=0}^{n} A_i S^i \quad (7)$$

$$F_S(W) = \sum_{n=0} A_i W^i \quad (8)$$

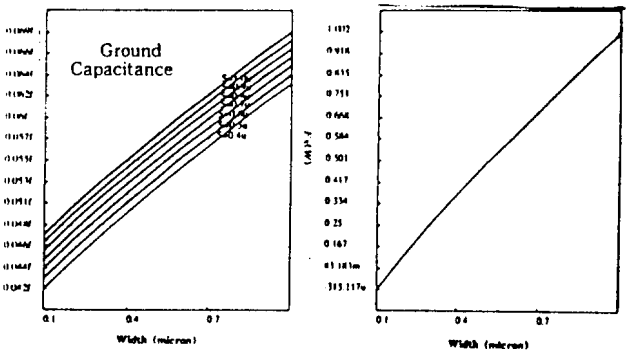
and their coefficients can be easily obtained by least square fit.

By adoping polynomial-based capacitance model for interconnect, the need for repetition of time-consuming numerical simulations are eliminated once the modelibraryis generated, leading to a capability of fast and accurate estimation of interconnect capacitances.



(a) (b)

Fig.3 (a) The dependence of coupling capacitance on the width of the wire in given range of space (b) The function, $F_s(W)$, depending on the space



(a) (b)

Fig.4 (a) The dependence of ground capacitance on the width of the wire in given range of space (b) The function, $F_s(S)$, depending on the space

B.Parametrization of parasitic inductance

The parasitic inductances in IC chips can be parametrized and modeled in the same way as described in the previous section. The inductance of an interconnect line is composed of the self inductance(L_s) induced by itself and the mutual inductance (L_m) induced by the neighboring interconnects. These inductances can be described as a function of layout parameters and technology parameters as well.

In the interconnect simulator used in the study, RAPHAEL, the inductance is calculated as follows:[5][6]

$$[L] = \frac{1}{c}[C]^{-1} \quad (9)$$

where [L] is inductance matrix, [C] is capacitance matrix and *c* is the speed of light.

As found in the analysis of simulation result for interconnect capacitance, it is found that the interconnect

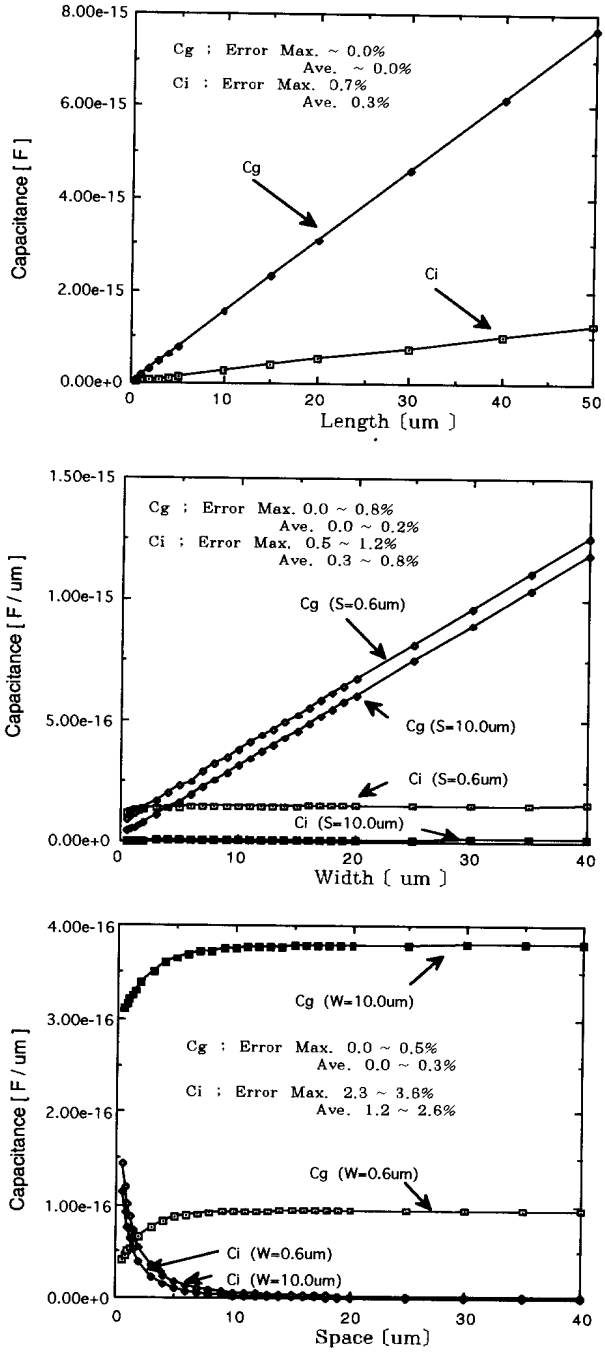


Fig.5 The fitting result for capacitance using SIMS (RAPHAEL vs SIMS)

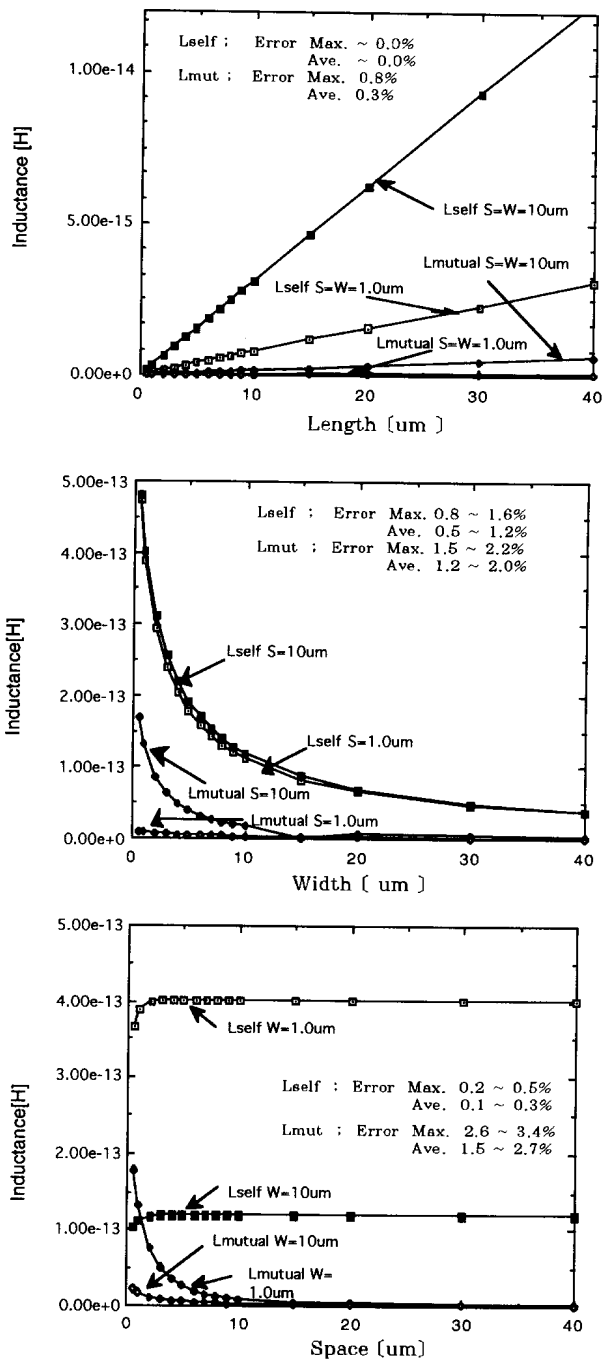


Fig.6 The fitting results for inductance using SIMS(RAPHAEL vs SIMS)

inductance is linearly proportional to the line length, but strongly nonlinear with line width and spacing. Therefore, basically the same methodology of developing analytic models as for interconnect capacitances is employed for interconnect inductances.

7. SIMULATION AND CURVE FITTING

Model library for parasitics is generated for each range of layout parameters using least square fit. A special care is taken for polynomial representation of strong nonlinear functions. It is seen in Fig.5, 6 that an excellent accuracy of model is obtained compared to the simulation results.

Dividing the spacing range into 3 subregions and the width range into 2 subregions results in the maximum fitting error less than 3%.

8. WIRE MODELING IN THE SCHEMATIC CAPTURE TOOL

Once the model library for interconnect parasitics is generated, circuit designers can access the library through the schematic capture tool in SIMS, which in turn creates netlist including the SPICE model for a particular interconnect pattern specified by the designer , automatically drives circuit simulator and display the circuit performance results through GUI. The designer, therefore, can analyze the effects of various interconnect patterns on his/her circuits in a very fast and accurate manner. Moreover, cross-talk can be simulated in the integrated modeling system by assigning separate ground nodes for different interconnect lines.

9. CONCLUSION

In this paper, an integrated design environment, SIMS, and related parameterized modeling of interconnect capacitances and inductances are presented. SIMS integrates numerical interconnect simulation with circuit simulation through a schematic capture tool. It not only preserves the accuracy of numerical simulations but also speed up the analysis by adopting parametrized parasitics modeling method based on interconnect simulations of various interconnect structures, opening wide the door to the design of circuit with optimized interconnect layout. Through the interface with a schematic capture tool, SIMS can simulate the effects of interconnect parasitics on circuit performances easily.

The delay due to interconnect in IC chips has emerged as one of the most critical factors in determining performances, and in this context, the capability of fast and accurate interconnect modeling and analysis provided by SIMS will ultimately make an important contribution to the realization of the concept of design for manufacturability and to the significant reduction in time-to-market for the benefit of design community.

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