TUTORIAL 4

DIGITAL CIRCUIT INTERCONNECT:
ISSUES, MODELS, ANALYSIS AND DESIGN

Speakers:

Ian Young, Intel Corp., Hillsboro, OR, *is a principal engineer in the Logic Technology Development Group at Intel Corporation. He is involved with the development of high speed CMOS and BiCMOS circuit design techniques, and interconnect and device modeling.*

Lawrence Pillage, University of Texas, Austin, TX, *is associate professor of electrical and computer engineering. He is best known for his work on moment-matching techniques (such as asymptotic waveform evaluation) for analyzing large interconnect circuit models.*

John Cohn, IBM Corp., Essex Junction, VT, *is a senior engineer with IBM's Electronic Design Automation group, where he is the lead architect for device-level layout automation. He is also adjunct professor at the University of Vermont.*

Background: This tutorial is intended for CAD developers and IC and system designers at various skill levels. Only a basic understanding of integrated circuits and circuit theory is assumed.

Description: Interconnect effects have a significant, sometimes dominant, impact on the performance of integrated circuits and systems. This tutorial begins by describing interconnect issues that must be dealt with during the design of integrated circuits. Considering today's top-down design methodology, algorithms and techniques are presented for modeling pre- and post-layout interconnect effects. This includes a complete survey of performance-driven interconnect design issues and algorithms.

Ian Young will begin by discussing the impact of submicron VLSI scaling on the interconnect delay and cross-talk problem, and the subsequent effect on the circuit design flow. In particular, he will describe the interconnect timing and signal integrity problems designers will be faced with for deep submicron multi-layer metal designs. Some of the circuit techniques that can be used to help minimize the detrimental effects of interconnect scaling and die-size increase will be presented. The role of interconnect resistance and capacitance estimation and layout extraction will be described, and where inductance may be a factor in circuit performance will also be considered.

Next, Larry Pillage will describe how to generate and analyze interconnect circuit models from the extracted parameters. RC and RLC lumped modeling approaches and assumptions will be described, along with efficient moment-matching techniques (e.g. AWE) for analyzing these circuits. Interfacing these reduced circuit models to transistor-level simulators and gate-level timing analyzers will be covered in detail. In addition to interconnect simulation and analysis, techniques for calculating performance gradients for the interconnect circuits will be described. These performance gradients can be used to drive gate sizing and interconnect synthesis.

John Cohn will then address all aspects of computer-aided interconnect and wiring design. Covering signal nets, clock trees, and power grids, he will describe how the parameters and models above are used to cope with interconnect effects in a top-down design flow environment. He will also discuss some of the ongoing design automation work for such problems, and will conclude by describing open problems in interconnect design and analysis.