TUTORIAL 2

DESIGN SOLUTIONS AND CHALLENGES FOR LOW POWER SYSTEMS

Speakers:

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Background: This tutorial is intended for both researchers and practitioners interested in the design of low power circuits and systems. Knowledge of integrated circuit design and familiarity with CAD tools for synthesis and layout will be helpful.

Description: In recent years, the desirability of portable operation of all types of electronic systems has become evident. One of the primary objectives in the design of portable systems is power reduction needed to minimize the size and weight allocated to batteries. Another driver of the progress in low power design is the increasing need to reduce active and/or standby power consumption in all electronic systems, low to high end, analog and digital. Essential elements of a low power design environment include means of analyzing the dissipation of a proposed or an existing design, mechanisms for minimizing the power consumption when needed and techniques to explore the impact of design trade-offs on the power consumption, area and performance of a design.

In this tutorial, techniques developed to address each of these issues will be described. The first part of the tutorial will analyze the sources of power dissipation in integrated circuits and will summarize the various power minimization approaches and techniques currently practiced in industry and academia. The second part will address methods for estimating, analyzing, and simulating power consumption at various abstraction levels: behavioral, functional, logic, switch and circuit. Special emphasis will be placed on the dependence of power consumption on signal statistics (transition probabilities and correlations) and delay models (zero-delay versus real-delay) and on how these can be addressed in the estimators and simulators. The efficiency and accuracy of the various approaches will be evaluated. In the third part, various approaches for power minimization at the algorithmic and architectural levels will be discussed, using transformations, architecture composition and hardware selection as the driving examples. Some mechanisms to reduce power consumption at the register transfer, logic and physical levels will be described (including low power techniques for state assignment, logic restructuring, technology mapping, placement and clock routing). Complications due to a real delay model which accounts for glitches will be addressed, and the effects of power minimization techniques on circuit area and performance will be described. Finally, reliability concerns and design-for-reliability will be discussed.

The tutorial will be illustrated with real life examples, taken from the design of a wireless, multi-media terminal ("The Infopad"), currently under development at the University of California, Berkeley. In addition, extensive experimental results on a representative set of benchmark circuits will be given in order to assess the efficiency and effectiveness of the power optimization techniques.