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CALL FOR PAPERS

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ELECTRON DEVICES SOCIETY

The 1995 INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN will be held November 5-9, 1995.
ICCAD is oriented towards Electrical Engineering CAD professionals, concentrating on CAD for Electronic Circuit Design.

AREAS OF INTEREST

Original technical papers on (but not limited to) the following topics are invited:

1) **COMBINATIONAL LOGIC SYNTHESIS:** Two-level and Multi-level logic optimization (area, timing, power). FPGA optimization. BDD techniques. Don't care methods. Technology mapping.
2) **SEQUENTIAL LOGIC SYNTHESIS AND VERIFICATION:** Sequential synthesis and optimization (e.g., state encoding, retiming) for area, timing, and power. Asynchronous design. Formal verification.
3) **HIGH-LEVEL SYNTHESIS:** Scheduling, allocation, and binding. Datapath and control synthesis. Memory system synthesis and optimization. Estimation, use of libraries, high-level synthesis environments.
4) **SYSTEM-LEVEL DESIGN ISSUES:** Specification, modeling and design of embedded systems. Hardware/software co-design. Software synthesis, analysis and verification. Interface synthesis. System integration and testability. Performance evaluation. Issues for real-time systems and DSP. ASIP synthesis.
5) **TIMING AND POWER MODELING AND ANALYSIS:** Modeling and analysis techniques for timing and power at the gate and higher levels of abstraction. False path analysis. Transparent latch timing analysis and clock schedule optimization.
6) **ANALOG SIMULATION AND SYNTHESIS:** Circuit, interconnect and timing simulation. Circuit-level delay, timing and power models. Analog circuit synthesis, optimization, and layout.
7) **CIRCUIT MODELS AND PROCESS DESIGN/TCAD:** Device models and interconnect parameters. Design for manufacturing. Equipment models and process and device simulation.
8) **DISCRETE SIMULATION:** Switch, logic and high-level modeling and simulation.
9) **ROUTING AND LAYOUT VERIFICATION:** Routing for ICs and packages. Performance-driven routing. DRC, ERC, circuit extraction and verification. Symbolic design and compaction.
10) **PLACEMENT AND FLOORPLANNING:** Partitioning, placement and floorplanning techniques. Area estimation. Module generation and leaf cell synthesis. Complete layout systems (e.g., full chip, MCM). Performance-driven techniques.
11) **BIST AND DFT:** Hardware techniques to improve testability for digital circuits and analog circuits. Analysis of BIST & DFT schemes. Partial and boundary scan.
12) **ATPG AND GENERAL TEST:** ATPG. New test strategies for digital circuits and analog circuits. Fault simulation.
13) **FRAMEWORKS AND CAD SYSTEMS:** Tool integration. Design representation. User interfaces. Databases. Design languages. CASE. Design planning and management. Complete CAD systems.

Author Information and Format

Authors should submit:

- 1 cover page including:
  - Title of paper.
  - The category 1 - 13 which most closely matches the papers content.
  - Complete name, return address, telephone number, fax number, email address and affiliation of each author.
  - Clear identification of the corresponding author.
  - **Papers will be reviewed anonymously. ONLY the cover page should identify the authors and their affiliations.**
- 10 copies of one page abstract
  - Abstract, typed on separate page should state clearly and precisely what is new and point out the significant results. The IMPACT, or potential impact, of the contribution will play a major role in evaluation.
- 10 copies of the completed paper not to exceed 20 pages, double-spaced, figures, tables and references included.
  - **Papers exceeding 20 pages or previously published will be returned to the authors.**

THIS INCLUDES WORKSHOP PROCEEDINGS.
For further information send a one-line email message to:
icpubpap@dac.com

- Authors should objectively address the significance of their contribution as demonstrated through theoretical advances, algorithmic/heuristic advances tested on "real" examples, and objective comparisons to existing techniques.

AUTHOR'S SCHEDULE

Deadline for submissions:	**Postmarked**	**April 10, 1995**
Notification of acceptance:		**July 5, 1995**
Deadline for final version:		**August 7, 1995**

Proposals for Panel Sessions and Tutorials are invited. Please send complete proposals including the participants to the address listed below.

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