A Comprehensive Fault Macromodel For Opamps

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Abstract

In this paper, a comprehensive macromodel for transistor level faults in an operational amplifier is developed. With the observation that faulty behavior at output may result from interfacing error in addition to the faulty component, parameters associated with input and output characteristics are incorporated. Test generation and fault classification are addressed for stand-alone opamps. A high fault coverage is achieved by a proposed testing strategy. Transistor level short/bridging faults are analyzed and classified into catastrophic faults and parametric faults. Based on the macromodels for parametric faults, fault simulation is performed for an active filter. We found many parametric faults in the active filter cannot be detected by traditional functional testing. A DFT scheme along with a current testing strategy to improve fault coverage is proposed.

I Introduction

Due to the trend of adopting complex analog circuits in ASICs, analog testing has gained more attention from researchers, designers and test engineers[1, 2, 3, 4, 10]. Analog fault simulation at the transistor level, in general, is computation-intensive. For complex circuits, the numerical non-convergence problem even makes the fault simulation totally fail. A viable approach is to partition a large analog circuit into functional blocks and replace each functional block with its macromodel. A macromodel is implemented with considerably fewer components or mathematical functions (behavioral model) to facilitate fault simulation. While we are concerned with simulation efficiency, it is also important that the macromodel should match the DC, AC and transient parameters of its transistor level counterpart. However, better match usually means enhanced complexity of macromodels and degraded simulation efficiency. While an analog component is imbedded in a large circuit, interfacing error due to loading effect should be properly modeled in its macromodel. If the parameters responsible for interfacing error are not incorporated, the faulty behavior we observe might come from the modeling error instead of physical defects.

The operational amplifiers are widely used in analog circuits. Many macromodels for the opamps have been proposed. The macromodels proposed in [5, 6] for fault-free opamps are comprehensive and an excellent match between macro level and transistor level has been achieved. However, these models are too complex for fault simulation. Simple macromodels proposed in [1, 2] benefit fault simulation but some important parameters for interfacing errors are not incorporated. For example, the dependence of output impedance on frequency is not modeled and, therefore, the accuracy of testing results may be significantly reduced. In this paper, we present a macromodel with accurate I/O parameters and poles/zeros addition to obtain the desired DC and AC responses. The fault macromodel can be imbedded in large circuits to overcome the fault simulation problem stated earlier.

A fault can be either catastrophic or parametric. Catastrophic faults will make the circuit completely out of function. A circuit with parametric faults, on the other hand, will still function but with degraded performance. Only parametric faults need to be considered for macromodeling. We investigate all transistor level short/bridging faults in an opamp. Even though the short/bridging fault list is huge, we will show that most of them are catastrophic and only a small number of faults require macromodeling.

For stand-alone opamps, we found that measuring *Vo_max** and *Vo_min** can detect a high percentage (>96%) of transistor level short/bridging faults. Based on this observation, we propose an efficient testing method for stand-alone opamps. The details will be discussed in Section III.

For circuits with embedded opamps, the fault macromodels we developed can be used for fault simulation and test generation. Our study has shown that many parametric faults are untestable when opamps in feedback configuration are embedded in an analog circuit. We use an active filter to illustrate. In [10], a DFT technique for active filters is proposed assuming only passive components external to opamps are faulty. Here, we consider faults inside opamps. An active filter is typically tested by functional testing, which sweeps the frequency of the input signal and observes the AC response at the output. Even for such an expensive testing approach which demands complex signal generators and long testing time, certain parametric faults cannot be tested. We therefore propose a DFT scheme to improve its testability. Under such a DFT scheme, measuring DC current will be sufficient to assure a high fault coverage for active filters. It may thus eliminate the need of expensive functional testing and the complex analog stimuli generation.

The rest of the paper is organized as follows. Section II describes the macromodeling procedure. Test generation and fault classification of the short/bridging faults in a stand-alone opamp are given in Section III. In Section IV, we use an active filter to demonstrate the effect of parametric faults on the functionality of a circuit with imbedded opamps. A current testing method and an associated DFT scheme are discussed.

II Macromodeling Procedure

The trade-off between circuit complexity and matching accuracy makes it impossible to incorporate all DC, AC and transient parameters in a single opamp. Our results show that it is very difficult to model some parameters simultaneously with certain accuracy. Considering the ease of testing vector generation and measurement, we take the DC and AC parameters as our testing parameters :

.DC -input offset voltage and current (*Vos*, *Ios*), input bias current (I_B), common mode input resistance (*Rcm*), output resistnce (*Ro_dc*),maximal output voltage (*Vo_max*), minimal output voltage (*Vo_min*) and power dissipation (*Pd*)

.AC -differential mode input resistance and capacitance (*Rid*, *Cid*), differential gain (*Avd*), 3db bandwidth (BW_{3db}), unit gain bandwidth (f_{0db}), output resistance (*Ro_ac*) and excess phase shift at unit gain ($\Delta\phi$)

We use the general purpose op741 as an example. The transistor level and macro level configurations are shown in Fig. 1(a) and 1(b) respectively. The macromodeling procedure is similar to the one proposed by Boyle et. al. [6] but our macromodel is simpler. This procedure can also be applied to the opamps implemented by MOS technology[9]. The input stage of the macromodel is similar to that proposed in [8]. The modeling procedure is summarized as follows:

1.Choose the parameters to be modeled (the DC and AC parameters above);

2.Simulate the transistor level opamp and obtain the values of the parameters;

3.Calculate the 'element value' in the macromodel through design equations;

4.Simulate the macromodel and obtain the values of the parameters (a new set of DC and AC parameters);

5.Obtain the error between 2. and 4. for each parameter.

6.Perform 'element value tweaking' and start from 4. if error is too large.

The advantage of this procedure is that it is fault-independent. That is, it can be applied for single/multiple faults, short/bridging/open/deviation faults, etc. Note that the structure of the macromodel is highly modular for the convenience of poles/zeros addition. The capacitor Cc models the frequency-dependency of output impedance and the location of the first pole. The excess phase shift $\Delta\phi$ is modeled by the module Rx/Cx. Modules Rp/Cp and Rz/Cz are used to adjust the location of the first pole if it can't be well modeled by Cc alone. Rpd is responsible for modeling DC power dissipation. VC/D1 and VE/D2 take care of *Vo_max* and *Vo_min* respectively. After the macromodel is obtained, it is not difficult to build a behavioral model. Some elements in the macromodel are used to perform certain functions and thus can be replaced directly by mathematical functions. For example, Ga, Ra, Cc and Gb in Fig. 1(b) correspond to the transfer function H(s) in its behavioral model version.

III Fault Analysis and Testing for Stand-alone op741

Physical defects at the layout level reflect themselves as two kinds of faults at the transistor level: catastrophic and parametric. A catastrophic fault makes the circuit completely out of function. For example, the output may be stuck at certain DC voltage level or the DC transfer characteristics may become very ill-behaved. A parametric fault results in the deviation of parameters, e.g., the magnitude of *Avd*. At the transistor level, the faults resulting from physical defects may be short, bridging, open, component value deviation in the active or the passive devices, etc. Here we consider short/bridging faults only.

A short fault is referred to as the faulty connection between any two nodes of a single device while a bridging fault denotes the faulty connection between any two nodes of different devices. For example, a three terminal device has 3 possible short faults and may involve in many possible bridging faults. A simple check shows that there are 25 nodes in the transistor level opamp in Fig. 1(a) and totally 300 short/bridging faults (59 are short faults and 241 are bridging faults).

Any of the AC or DC parameters can be used for fault detection. It is intuitive to infer that when a short/bridging fault occur inside an opamp, the DC voltage level at certain nodes should be changed. The faulty DC voltages should affect some DC parameters in the macro level. After investigation, we found parameters *Vos*, *Vo_min* and *Vo_max* are useful for detecting most of the transistor level faults.

The DC parameters *Vos*, *Vo_min* and *Vo_max* for a stand-alone, open-loop op741 can be derived as follows. We connect the node 'V-' to ground and apply DC voltages sweeping from '-15v' to '+15v' at the node 'V+' to obtain *Vo_min* and *Vo_max*. *Vos* can be obtained by observing the output voltage when the opamp is in source follower configuration (connecting 'V-' and 'output' together) with 'V+' grounded. We need to know the nominal values as well as the *ranges* of these parameters for circuits considered to be fault-free. The nominal (fault-free) values for the three parameters are *Vos* = -1.40mv, *Vo_max* = 14.60v and *Vo_min* = -13.08v. For a manufactured opamp, *Vos* consists of two parts: *Vos_system* and *Vos_random*. *Vos_system* is due to the unsymmetrical schematic (in our example, Q5 in the differential stage) while *Vos_random* is due to the random mismatch between transistors and resistors in the differential stage. The nominal value '-1.40mv' comes from *Vos_system* because we are not considering device mismatch during simulation. Refer to [7] and assume the standard deviation of resistor matching is 1%, that of Is (transport saturation current) matching is 5%, and that of β (current gain for the PNP transistor) matching is 10%, we obtain the standard deviation of *Vos_random* = 2.73mv (our β = 10 and the collector current Ic of Q3 and Q4 = 7.7uA). Thus, under our assumption, *Vos* is a Gaussian random variable with μ (mean) = -1.40mv and σ (standard deviation) = 2.73mv. Therefore, the probability '*Vos* > 6.79mv ($\mu + 3\sigma$) or *Vos* < -9.59mv ($\mu - 3\sigma$) for a fault-free op741' is less than 0.3%. Therefore, we assume that if *Vos* of the opamp under test does not fall into this range, it is faulty. For simplicity, we consider [-10mv, 10mv] as the fault-free range, instead of [-

9.59mv, 6.79mv]. For *Vo_min* and *Vo_max*, we consider deviation from the nominal value larger than '0.1v' as defective.

Our testing procedure is summarized as follows. For the op741 in the same configuration as we did earlier for obtaining *Vo_min* and *Vo_max*, apply two DC voltage '-10mv' and '10mv' to the node 'V+'. The corresponding output is denoted *Vo_min** and *Vo_max**. If either one of the conditions happens, the opamp is declared as faulty:

1. *Vo_max** < *Vo_max* - 0.1v or *Vo_max** > *Vo_max*+ 0.1v;
2. *Vo_min** <*Vo_min* - 0.1v or *Vo_min** > *Vo_min* + 0.1v;
3. *Vos* >10mv or *Vos* < -10mv;

Note that the first two conditions implicitly include the third one and it will be sufficient just to compare (*Vo_min**, *Vo_max**) with (*Vo_min*, *Vo_max*). Because the gain of the op741 is very high, the width ΔV of the transition region in DC transfer curve is about 30v / *Avd* = 2mv and the transition region falls between '-0.40mv' and '-2.40mv'. Therefore, condition 3 is implied by conditions 1 and 2 and is redundant. Thus, the values of *Vo_min* and *Vo_max* for fault-free opamps are identical for the input '-10mv', '10mv' and sweeping from '-15v' to '15v'.

We measure *Vo_min** and *Vo_max** for short/bridging faults in a op741. Out of 300 faults, 289 can be detected (a fault coverage of 96.3%) by measuring these two parameters. The 11 undetected faults are *R11 short*(F1), $Q22_{BE}$ *short*(F2), *R6 short*(F3), $Q6_C/Q22_B$ *bridging*(F4), $Q7_E/Q22_B$ *bridging*(F5), $Q6_E/Q22_B$ *bridging*(F6), $Q16_E/Q22_B$ *bridging*(F7), $Q11_E/Q16_E$ *bridging*(F8), $Q11_E/Q22_B$ *bridging*(F9), $Q6_E/Q7_E$ *bridging*(F10) and *R4 short*(F11). The subscript *B,C* and *E* stands for the base, collector and emitter respectively. Note that 5 out of the 11 faults involve the bridging of node Q22*B* with other nodes. Note that the probability of occurrence of these 5 faults can be reduced if we place node $Q22_B$ distant from the 5 associated nodes in the layout.

We examine other macro level parameters for these 11 undetected faults. Many of them can be detected by other parameters. Referring to Table 1, the parameter BW_{3db} can detect F3, F7, F8, F9 and F11. The testing vector is a sinusoidal signal with frequency equal to the 3db bandwidth of the fault-free opamp. The parameter *Ro_ac* can detect F1, F2, F8 and F11 and the testing vector is an sinusoidal AC current applied at the output with both inputs grounded. After testing parameters BW_{3db} and *Ro*_ac, F4, F5, F6 and F10 remain undetected.

For opamps embedded in a circuit, direct measurement of *Vos, Vo_min* and Vo_max** is not possible. To investigate how the short/bridging faults inside opamps affect the performance of opamps-imbedded circuits, we first use the following simple criterion to classify the 300 transistor level faults: if *Vo_max* > 1.0v and *Vo_min* < -1.0v, the fault is classified as parametric. Otherwise, it is considered as catastrophic. Based upon this simple criterion, we found 67 faults are parametric and 233 are catastrophic. Note that 56 of these 67 parametric faults can be detected by measuring *Vo_max** and *Vo_min** if the opamp is stand-alone. Another very important information is that, 45 out of the 67 parametric faults have *Vos* < -10mv or *Vos* > 10mv and the *Vos* for all catastrophic faults are very different from the nominal *Vos.*

Steps 1 - 6 in Sec. II are applied to these 67 parametric faults for macromodel generation with configuration shown in Fig. 1(b). Each parametric fault corresponds to a macromodel. The simulation results for some sample parametric faults are shown in Table 2. Each column corresponds to either the good or a faulty opamp and each row corresponds to a modeled parameter. Parameter values at transistor level are shown on the top of the values at the macro level. The values for I_B *(*82.2nA*), Rid*(3.63Gohm), *Cid*(1.29pF) and *Rcm*(0.90Gohm) are essentially identical for all faults listed in Table 2. Fig. 2(a) shows that the output impedance is frequency-dependent for the good and faulty opamps. This parameter is important when AC testing is performed for opamps-imbedded circuits. In Fig. 2(b), the macromodel for the good opamp is verified by adding feedback and loading effect to provide similar condition when the opamp is embedded in a large circuit.

IV A 1KHz Active Filter and the DFT Scheme

The results in Sec. III show that 56 of the 67 parametric faults can be easily detected in the stand-alone op741. We use an active filter implemented with op741 macromodels (Fig. 3) to demonstrate the effect of these faults when opamps are imbedded in a circuit. The active filter can perform high pass, low pass and band pass function with 1KHz bandwidth. For simplicity, assume the faults occur in opamp X2 and only one fault occurs at one time. Also, assume no bridging faults occur between the nodes in different opamps. We first examine the quality of functional testing (sweeping the frequency) regarding its capability of detecting these 67 parametric faults. We found less than 25% of parametric faults can be detected by exhaustive functional testing. This is because the AC response of a feedback opamp depends mainly on the feedback components if the open-loop gain of the opamp is large enough. That is, the opamp is desensitized in a feedback configuration which results in the reduction of testability of opamps. Similar (low) coverage is observed for faults in X1 and X3.

Due to the low fault coverage of functional testing, we propose a non-functional testing approach that measures the current Icc flowing out of Vcc. Measuring the current Icc can detect 27 out of the 67 parametric faults (a fault coverage of 40.3%). This coverage, though low, is higher than that of exhaustive functional testing. Note that in both approaches, an active filter is declared faulty if the measured error exceeds 10% of the nominal value (the nominal value for Icc is 18.02mA).

The fault coverages of both functional testing and current testing are far from satisfactory. We, therefore, propose a DFT scheme for such active filters to increase the testability of embedded opamps. In Fig. 3, the highlighted lines are added DFT circuit. We add 6 switches (S1 - S6), 3 resistors (Rx1 - Rx3), 3 output pins (P1 - P3) and 1 control pin (Vt) to the active filter. Each switch is implemented with a simple BJT as shown on the upper left corner of the figure. All switches are

open (Vt = 0v, transistors are 'OFF') in functional mode and are closed (Vt = 0.85v, transistors are 'ON') in testing mode. The 'ON' resistance of the non-ideal switch is about 100 ohm. After multiplied by the input biasing current I_B = 82.2nA, the finite voltage drop introduced is less than 10μv. In testing mode, each opamp is configured as a source follower. If all the opamps are stand-alone, the voltage at the output of opamp X1, X2 and X3 will be -*Vos_x1*, -*Vos_x2* and -*Vos_x3*. Note that the output resistance of a source follower is very small due the negative feedback effect (in our example, the output resistance is about 0.05ohm (*Ro_dc/Avd*) for the fault-free opamp). Even for faulty opamps, the output resistance is very unlikely to become comparable to the external resistance seen by the output node. The above argument indicates that -*Vos_x1*, -*Vos_x2* and -*Vos_x3* will remain almost the same regardless the opamps are stand-alone or imbedded. That is, in source follower configuration, the opamps are essentially isolated from each other without 'cutting' the existing lines. If we place a 10 ohm resistor Rx between the output of opamp X and ground, the current Ix flowing through Rx is approximately -*Vos_x*/Rx because 10 ohm is still much larger than *Ro_dc/Avd*. For the good opamp, Ix is about '0.14'mA. For most of the faulty opamps, Ix will be either greater than '1mA' or smaller than '-1mA'. It is natural to assign '1mA' as our criterion for fault detection. Also, the non-ideal switch has almost no effect on our DFT scheme because 10μv is much less than the nominal |*Vos*|.

Simulation results show the current Icc flowing out of Vcc for the fault-free active filter, under testing mode, is '18.13mA' and the total current I_{TEST} flowing through Rx1, Rx2 and Rx3 (with P1, P2 and P3 connected to ground) is '0.42mA'. For the 67 parametric faults, 56 (83.5%) can be detected by measuring Icc and I_{TEST} . All 233 catastrophic faults can also be detected in this manner. The overall coverage for faults in X2 is then increased to 96.3% (289/300). The fault coverage figures are about the same for faults in X1 or X3 because of the 'isolation' property of our DFT scheme.

The area overhead, counting the transistors only, is about 6/66 = 9.1%. The functionality remains almost unchanged as indicated by our simulation results. The gain error at 1KHz is less than 0.01%. Here we assume the 3 extra pad capacitance (the 3 capacitors boxed by highlighted lines) introduced by the 3 output pins is 5pF. It is also possible to replace the resistors Rx1, Rx2 and Rx3 with three 'voltage controlled' resistors implemented by BJT and merge the 3 output pins into one. The disadvantage of this scheme is that each resistor may need 2 BJTs to achieve the desired linearity. The area overhead will then increase but we may save 2 pins and no extra pad capacitance is introduced. When many opamps are involved in a circuit, 'voltage controlled' resistors are preferred because of the constant extra pin count.

V Conclusions

A comprehensive fault macromodel for opamps is proposed. The parameters incorporated in the model are selected by taking the interfacing errors and simulation efficiency into account. The procedure for generation of the macromodel is described. All possible 300 short/bridging faults in the stand-alone op741 are investigated. A very simple DC testing strategy that measures *Vo_min** and *Vo_max** for a stand-alone op741 can achieve a fault coverage of 96.3%. We further classify the 300 faults into 67 parametric faults and 233 catastrophic faults according to *Vo_min* and *Vo_max* in the macro level. The macromodels corresponding to parametric faults are used in an active filter for fault simulation. For those parametric faults, we found that the fault coverage of exhaustive functional testing is less than 25%. We have proposed a current testing strategy. By employing a novel DFT scheme that connect all opamps in source follower configuration in the test mode, the current testing method dramatically increases the fault coverage.

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Table 1: The parameters that detect the 11 parametric faults (×)

	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11
Avd			×					×			×
Δϕ											
BW_{3db}			×				×	×	×		×
f_{0db}								×			×
Ro_dc	×		×					×			×
Rin, Cin				×							
Pd	×										×
Ro_ac	×	×						×			×

Table 2: Opamp parameters (transistor level/*macro level*)

	good	fault#1	fault#2	fault#3	fault#4	fault#5	fault#6
DC parameters							
Vos (mv)	-1.400	-1.490	-1.400	-1.130	-1.560	-14.710	101.060
	-1.400	*-1.490*	*-1.400*	*-1.130*	*-1.560*	*-14.710*	*101.060*
Ios (nA)	-1.0	-1.0	-1.0	-1.0	-1.0	-11.5	62.2
	-1.0	*-1.0*	*-1.0*	*-1.0*	*-1.0*	*-11.5*	*62.2*
R_{o_dc} (ohm)	807	938	808	688	1210	731	755
	807	*938*	*808*	*688*	*1209*	*730*	*754*
Vo_max (V)	14.60	14.60	14.60	14.60	14.60	14.62	14.12
	14.61	*14.61*	*14.61*	*14.60*	*14.60*	*14.62*	*14.13*
Vo_min (V)	-13.08	-13.13	-13.02	-13.16	-12.70	-13.08	-13.08
	-13.08	*-13.12*	*-13.02*	*-13.16*	*-12.69*	*-13.08*	*-13.08*
Pd (mW)	180.0	228.3	180.0	179.0	500.0	180.0	180.0
	180.0	*229.9*	*180.0*	*180.0*	*501.0*	*180.0*	*180.0*
AC parameters							
Avd (e4 HZ)	1.585	1.448	1.584	1.828	1.596	2.005	0.641
	1.577	*1.448*	*1.583*	*1.818*	*1.606*	*2.010*	*0.637*
Δϕ (deg) @Avd=1	6.1	4.7	6.1	3.9	6.9	7.6	3.2
	6.0	*4.6*	*6.0*	*3.9*	*6.8*	*7.6*	*3.2*
BW_{3db} (HZ)	53.0	55.0	50.1	43.7	61.3	52.0	47.5
	51.2	*55.0*	*50.1*	*41.6*	*63.1*	*52.2*	*47.5*
f_{0db} (e5 HZ)	8.100	7.950	7.950	7.950	7.943	10.715	3.091
	7.943	*7.943*	*7.943*	*7.943*	*7.850*	*10.805*	*3.080*
R_{o_ac} (ohm) @10KHZ	28.2	16.2	21.7	28.3	13.5	28.3	28.5
	28.9	*17.2*	*29.0*	*22.2*	*14.8*	*26.0*	*26.5*

fault#1: R11 short fault#3: R6 short fault#5: R3 short
fault#2: $Q22_{BE}$ short fault#4: R9 short fault#6: $Q7_{BE}$ short

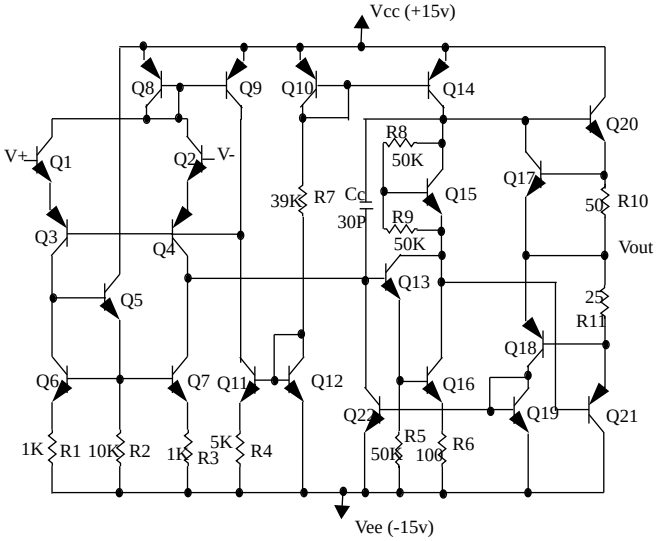

Fig. 1(a) Transistor level circuit diagram for op741

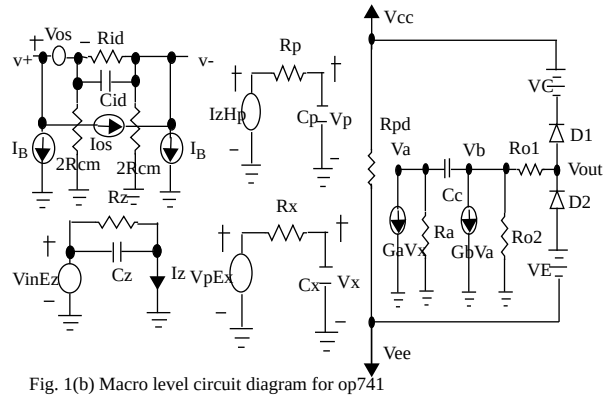

Fig. 1(b) Macro level circuit diagram for op741

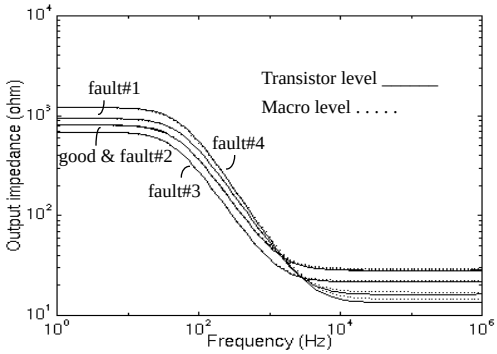

Fig. 2(a) The dependence of output impedance on frequency

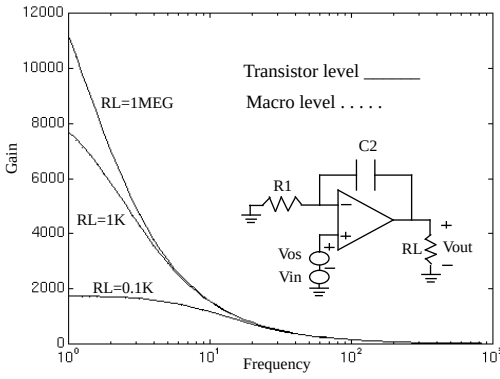

Fig. 2(b) Frequency response of op741 with feedback and loading

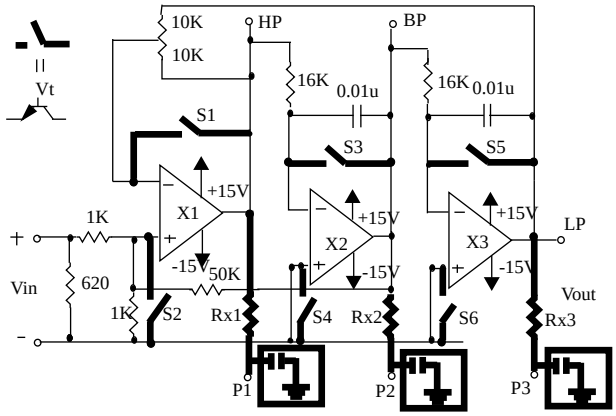

Fig. 3 A state variable active filter