Analytical Fault Modeling and Static Test Generation for Analog ICs †

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Abstract

Static tests are key in reducing the current high cost of testing analog and mixed-signal ICs. A new DC test generation technique for detecting catastrophic failures in this class of circuits is presented. To include the effect of tolerance of parameters during testing, the test generation problem is formulated as a minimax optimization problem, and solved iteratively as successive linear programming problems. An analytical fault modeling technique, based on manufacturing defect statistics is used to derive the fault list for the test generation. Using the technique presented here an efficient static test set for analog and mixed-signal ICs can be constructed, reducing both the test time and the packaging cost.

1: Introduction

Analog and mixed-signal ICs have been traditionally tested by verifying a subset of the design specifications. In general, specification (or functional) testing procedures are time consuming and not economical. Further, each design may require a unique test equipment. A testing procedure based on an analog fault model is required to ease this bottle-neck in testing mixed-signal ICs.

1.1: Previous work in analog testing

In [1,2] attempts have been made to develop analog fault models by performing a Monte-Carlo defect simulation. In [1] it was suggested that the faulty analog behavior be modeled as modifications to the nominal macromodel. The drawback with this approach is that the faulty macromodel may require a large number of components, defeating the purpose of macromodeling. Further, the procedure outlined does not lend itself to automation. The consensus from these initial studies is that failures in analog systems can be classified into two main categories:

1. Parametric faults resulting in functional circuits with degraded specifications.
2. Catastrophic faults resulting in complete absence of the desired function.

Various authors have addressed the issue of testing for the above two classes of faults. In [3] an algorithm was presented to obtain an optimal functional test set for the detection of parametric faults. In [5] the test generation problem for detecting parametric faults in linear analog circuits is cast as a quadratic programming problem. Here, the correlation between the faults and the defects is not clear. Also, the practicality of using a quadratic objective function has not been proven. In [6] a search technique in the frequency domain is used to determine test frequencies for a given set of faults. But, the authors do not address the issue of tolerance of parameters in their test generation procedure. In [7] a DC test selection procedure was presented where the detection criteria included the effect of tolerance of parameters but, a linear approximation around the nominal values was used.

1.2: Our contribution

DC testing is most suitable to be performed at the wafer probe stage and an efficient test procedure at this stage will result in the rejection of many obviously faulty chips, decreasing the cost of packaging. In this paper, we focus on developing a static fault model and an associated test strategy for detecting catastrophic failures in analog and mixed-signal systems.

Static testing is specially useful in a large class of circuits for which failures in the circuit result in changes in the DC signal values at the primary outputs. Also, with the use of DFT techniques in mixed-signal designs[10], it is possible to control and observe analog macros in isolation. Thus an efficient static test set at the macro level needs to be developed to reduce the cost of testing. Analog test generation in its simplest form can be viewed as finding an input which maximizes the error between the good and the

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faulty circuit. But, the variability in the process may counteract rendering this maximization inadequate. In this paper we show that to include the effect of tolerance in parameters, the test generation problem may be formulated as a minimax optimization problem. Since this problem in general is nonlinear, an iterative procedure is employed wherein a linear programming subproblem is solved at each iteration. Further, to obtain accurate estimates for fault coverage, we present an analytical method to derive probabilities for the faults using the manufacturing defect statistics and the nominal layout.

2: Analytical Fault Modeling

Common figures of merit such as fault coverage, test set size etc. are accurate to the extent the fault model represent the underlying physical disturbances. Since most of the current mixed-signal designs have evolved by fabricating the analog blocks in existing digital processes, it is reasonable to expect similar defect causing mechanisms to be active both in the analog and the digital portion of the die. Previous studies[9] in digital circuits indicate that lithographic and pinhole defects are the primary cause of yield loss in digital circuits and their defect statistics can be described by the following two distributions:
1. Defect size distribution 2. Defect Spatial distribution.
We use the model proposed in [4] for the defect size distribution and the models proposed in [8] for the spatial distribution. Since the analog macrocell under consideration is usually a small fraction of the total chip area, the defects are assumed to be uniformly distributed on the macrocell. A defect landing in those areas of the mask where there is no useful circuit information does not cause any circuit failure and hence can be neglected. Once the defect sensitive areas of the cell are identified, the total probability of a defect causing a failure in the sensitive area is given as,

$$p_d = \int_{D_{min}}^{D_{max}} h(y)\frac{A(y)}{A_{cell}}dy \qquad \text{(EQ 1)}$$

where *h(y)* is the defect size distribution, *A(y) is* the sensitive area for the pattern under consideration and A_{cell} the area of the macro. The limits of integration D_{max} and D_{min}- the maximum and minimum defect diameters respectively- are obtained from the design rule specifications. If N_c is the total number of defects on chip it can be shown that the probability of no failures in the sensitive area is given as,

$$\overline{P}_f = \sum_{i=0}^{N_c} \left(1 - p_d\right)^i P_i \qquad \text{(EQ 2)}$$

Here P_i is the probability of *i* defects landing in the macrocell and is obtained by using a procedure outlined in [8]. Thus the probability of a failure in the sensitive area is given by,

$$P_f = 1 - \overline{P}_f \qquad \text{(EQ 3)}$$

The above relations are repeatedly used for each sensitive area in every mask layer and the associated probabilities computed. To each failure in the layout pattern there corresponds a circuit-level structural failure which is assigned the probability just derived for the sensitive area.

3: Test generation and minimax criterion

Faulty analog circuits with catastrophic defects may be highly sensitive to process variations and for certain inputs may display good behavior locally. Any effective test strategy should resolve such local equivalences between the good and the faulty circuits. Consider a non-linear circuit described by,

$$y_g = g(\boldsymbol{x}, \boldsymbol{p}) \qquad \text{(EQ 4)}$$

$$y_f = f(\boldsymbol{x}, \boldsymbol{p}) \qquad \text{(EQ 5)}$$

where,

$\boldsymbol{x}$- a n_I dimensional vector of inputs.

$\boldsymbol{p}$- a n_p dimensional vector of process parameters.

y_g- the output for the good circuit.

y_f- the output for the faulty circuit.

Any test input generated should detect a fault for the worst case of the process variation. Since the output is nonlinearly related to both the inputs and the parameters, determining the worst case of the process deviation is a non-trivial task and cannot be simply obtained by setting the process parameters to their upper and lower bounds. Rather we need to pick through an optimization procedure, those values of the process parameters which will cause the faulty and good circuits to behave as close to each other as possible and then find the corresponding input vector which will detect the fault for this worst case. For ease of notation we denote,

$$y_g - y_f = E(\boldsymbol{x}, \boldsymbol{p}) = g(\boldsymbol{x}, \boldsymbol{p}) - f(\boldsymbol{x}, \boldsymbol{p})$$

For each fault, the objective is to maximize the magnitude of the error $E(\boldsymbol{x}, \boldsymbol{p})$ for the worst case value of $\boldsymbol{p}$. This problem can be formulated as a minimax optimization problem as follows,

$$\min_{\boldsymbol{p} \in P} \max_{\boldsymbol{x} \in X} |E(\boldsymbol{x}, \boldsymbol{p})|$$

The set *X* represents the physical limits to the test inputs which can be applied whereas the set *P* contains the

bounds on the process parameters, typically specified by process engineers. The above problem can be solved iteratively by using a procedure shown below.

3.1: Numerical Implementation

The set P typically has a higher dimension than X and to reduce the numerical complexity we discretize set X. Using an iterative procedure to solve the optimization problem, the resulting discretized problem becomes,

$$\min_{p \in P} \max_{i=1\ldots N} \left| E_i(\boldsymbol{p_k}) + \langle a_i(\boldsymbol{p_k}), \boldsymbol{p} - \boldsymbol{p_k} \rangle \right|$$

Here $a_i(\boldsymbol{p_k})$ is the gradient vector at $\boldsymbol{p_k}$ and $\langle\ ,\ \rangle$ denotes the inner product operation. The discretization of set X physically corresponds to a finite element division of the input space. The gradient and objective function values at $\boldsymbol{p_k}$ are obtained by using a piecewise linear model, constructed by DC simulations.

In the form stated above, the minimax problem is a non-smooth optimization problem. By introducing an additional variable γ the nonlinearities can be removed and the new problem can be rewritten as,

$\boldsymbol{min}\ \gamma$

satisfying,

$$E_i(\boldsymbol{p_k}) + \langle a_i(\boldsymbol{p_k}), \boldsymbol{p} - \boldsymbol{p_k} \rangle \le \gamma,\ i=1..N$$

$$p_j^L \le p_j \le p_j^H,\ j=1..n_p$$

$$0 \le \gamma \le 2\left|\gamma_{max}\right|$$

Here γ_{max} is the physical limit to the maximum error.

The above problem is a linear programming(LP) problem and rapid algorithms exist to solve such problems. If $\overline{\boldsymbol{P}}_k$ solves the LP problem at iteration k, then the guess for next iteration k+1 is given by, $\boldsymbol{p}_{k+1} = \boldsymbol{p}_k + \lambda_k \boldsymbol{d}_k$ where, $\boldsymbol{d}_k = \overline{\boldsymbol{P}}_k - \boldsymbol{p}_k$ gives the descent direction and λ_k, the step taken along the descent direction. The nominal process vector $\boldsymbol{p_o}$ is used as the initial guess for the solution. The iterations are continued until $\left\|\boldsymbol{p}_{k+1} - \boldsymbol{p}_k\right\| \le \varepsilon$, where ε is the required precision for the solution vector. The solution to this problem gives the worst case parameter vector and also the input vector (denoted by $\bar{\boldsymbol{x}}_t$) which maximizes the difference between the outputs for the good and faulty circuits. The optimal value of γ, say $\bar{\gamma}$, gives the maximum possible difference between the good and the faulty circuits which can be excited by $\bar{\boldsymbol{x}}_t$ in the worst case. If the value of $\bar{\gamma}$ is less than a threshold- determined by the resolution of the measurement system- then the fault cannot be detected. Once the test input($\bar{\boldsymbol{x}}_t$) for the fault under consideration has been determined, for a go/ no-go testing decision, bounds on the output for the good circuit under the test input excitation need to be determined. For a test excitation $\bar{\boldsymbol{x}}_t$, and output measurement x_o, the circuit is non-faulty if and only if,

$$x_o^{min} \le x_o \le x_o^{max}$$

where, $x_o^{min} = min\{ g(\bar{\boldsymbol{x}}_t, \boldsymbol{p}) \}$ and $x_o^{max} = max\{ g(\bar{\boldsymbol{x}}_t, \boldsymbol{p}) \}$. For the simplifying assumption of an affine approximation around the nominal process values the detection criteria of [7] is equivalent to a single linear programming step in our method. The additional advantage of this method is that the faulty signatures in the measurement space are not explicitly constructed and stored. Further, by using this method and employing the interior-point methods for linear programming, polynomial time behavior may be achieved.

4: Results

We have applied the procedure outlined in this paper to a CMOS two-stage comparator shown in Fig.1 designed for the 2μ-MOSIS process. The defect statistics from [9] were used to generate the fault probabilities. If the procedure of introducing shorts and opens at the devices [7] were used with 5 faults per transistor, then the number of faults in the fault list would be 45. By following the analytical procedure presented here of probing the sensitive areas, the number of faults has been reduced to 29, a reduction of 36%, which can be attributed to the fact that a maximum defect diameter constraint was used, resulting in zero probability for a number of faults. A sample from this reduced fault list with probabilities of failure, is shown in Table 1. For this example, we have considered variations in zero-bias threshold voltages.To illustrate the effect of tolerance on the detectability of the test set we show in Fig.2 the transfer curve of the comparator for the case of the good circuit and also for the case of the faulty circuit (6-4 short). Without any process variation, this faulty circuit could be detected by applying any input voltage within the range 0-1V. However, considering a threshold voltage variation (0.6-1.1V) for the NMOS transistor (nominal value is 0.934V), it can be seen that the faulty circuit behaves like a good circuit for voltages between 0.5-1.0V. Thus the range over which the fault can be detected has been reduced to 0-0.5V. The transfer curve for the good comparator is robust and showed little change for this variation of threshold voltage.

The transfer curve of a comparator is typically verified by grounding the negative input of the comparator and sweeping the positive input through the allowable range. As a first experiment, we set the negative input to ground and seek the test input voltages at the positive input. Applying the test generation procedure presented here to the list of faults we find that the final test set had just 4 test

inputs namely 0.4V, +2.5V, -2.5V and -0.3V. The faults such as short between 7&6 and the short between 4 &10 remain undetected. We performed a second experiment by letting the negative input(V-) also to be a variable in the test generation procedure. Using the minimax procedure we find that test generation was successful for the short between node 6&7. The test inputs were -0.6V and -1.2V for the V^+ and V^- inputs respectively. This fault would have passed the traditional specification test of verifying the transfer curve of the comparator although, it would have been detected by a CMRR(common-mode rejection ratio) test which is an expensive test. The short between nodes 4&10 remains undetected. Thus, by using the test procedure presented here a small static test set with high fault coverage can be constructed eliminating the need for costly specification tests.

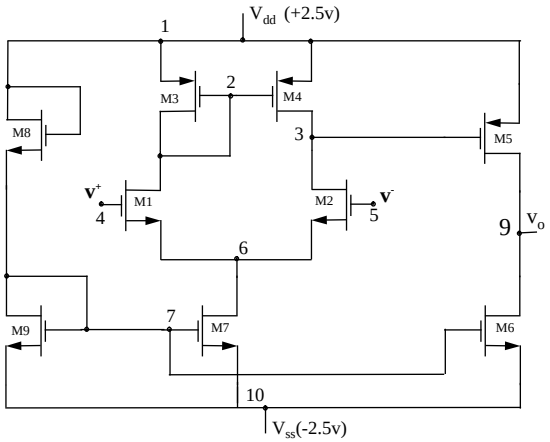

Fig.1: Two Stage comparator

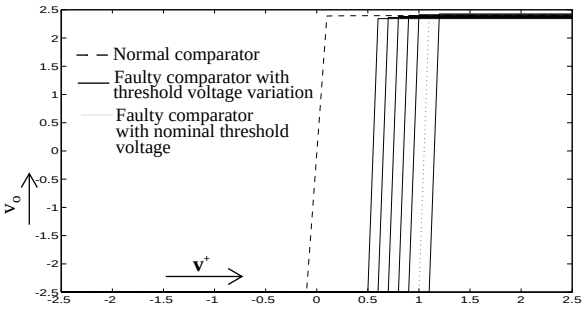

Fig.2: Transfer curves with threshold voltage variation

Table 1: Sample list of faults

Fault Type	Probability
Nodes 4 and 6 short	8.2918e-4
Nodes 4 and 10 short	0.0012
Nodes 9 and 3 short	8.8293e-4
Nodes 6 and 7 short	6.5629e-4
Nodes 7 and 9 short	7.4858e-4
M5 drain open	9.5251e-4
M7 source open	0.0012
M4 drain open	0.0012

Table 2: Test inputs for the faults in Table 1

Fault Type	Inputs		Error value	Output bounds of the good circuit
	V^+	V^-		
Nodes 4&6 short	0.4V	0	4.8959V	[2.39, 2.45]
M7 source open	-2.5V	0	5.0V	[-2.5,-2.5]
Nodes 9&3 short	-2.5V	0	3.6683V	[-2.5,-2.5]
Nodes 7&9 short	2.5V	0	1.3713V	[2.39, 2.45]
M4 drain open	-0.3V	0	4.9071V	[-2.5,-2.5]
Nodes 4&10 short	none	none	0	no test
M5 drain open	2.5V	0	0.0038V	[2.39, 2.45]
Nodes 6 &7 short	-0.6V	-1.2V	4.89V	[2.43,2.47]

5: Conclusions

We have presented a new approach for the DC test generation for analog ICs. To include the effect of tolerance of parameters, the test generation problem was formulated as a minimax optimization problem. We have demonstrated the utility of our approach by applying the procedure for a CMOS comparator and have found that, by the judicious choice of a small number of static tests, most of the faults may be detected. This procedure is currently being studied for larger circuits such as A/D converters.

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