

ASP-DAC 2008 Technical Program Committee

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Nat'l Tsing Hua Univ., Taiwan

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Seoul Nat'l Univ., Korea

TPC Subcommittee

(*indicates subcommittee chair)

[1] System Level Design

Methodology

*Sri Parameswaran

Univ. of New South Wales,
Australia

Eui-Young Chung

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Univ. of California, Irvine, USA

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CEA-LETI, France

Jean Christophe Madre

Synopsys, France

Tulika Mitra

Nat'l Univ. of Singapore,
Singapore

Tsuneo Nakata

Fujitsu Lab., Japan

[2] Embedded and Real-Time Systems

*Hiroyuki Tomiyama

Nagoya Univ., Japan

Naehyuck Chang

Seoul Nat'l Univ., Korea

Karam S. Chatha

Arizona State Univ., USA

Pai Chou

Univ. of California, Irvine, USA

Maziar Goudarzi

Kyushu Univ., Japan

Tei-Wei Kuo

Nat'l Taiwan Univ., Taiwan

Paolo Ienne

EPFL, Switzerland

Yunheung Paek

Seoul Nat'l Univ., Korea

Sungjoo Yoo

Samsung Electronics, Korea

[3] Behavioral/Logic Synthesis and Optimization

*Shinji Kimura

Waseda Univ., Japan

Shih-Chieh Chang

Nat'l Tsing Hua Univ., Taiwan

Deming Chen

Univ. of Illinois, Urbana-
Champaign, USA

Ki-Seok Chung

Hanyang Univ., Korea

Hiroyuki Higuchi

Fujitsu Lab., Japan

Taewhan Kim

Seoul Nat'l Univ., Korea

Yuan Xie

Penn. State Univ., USA

[4] Validation and Verification for Behavioral/Logic Design

*Jin-Young Choi

Korea Univ., Korea

Thomas Kropf

Bosch, Germany

Hee Hwan Kwak

Posdata, USA

Igor Markov

Univ. of Michigan, USA

Shin'ichi Minato

Hokkaido Univ., Japan

Miroslav Velez

Consultant, USA

Farn Wang

Nat'l Taiwan Univ., Taiwan

[5] Physical Design (Routing)

*Martin D. F. Wong

Univ. of Illinois, Urbana-
Champaign, USA

Charles Chiang

Synopsys, USA

Sung Kyu Lim

Georgia Inst. of Tech., USA

Hyunchul Shin

Hanyang Univ., Korea

Atsushi Takahashi

Tokyo Inst. of Tech., Japan

Ting-Chi Wang

Nat'l Tsing Hua Univ., Taiwan

[6] Physical Design (Placement)

*Yao-Wen Chang

Nat'l Taiwan Univ., Taiwan

Wai-Kei Mak

Nat'l Tsing Hua Univ., Taiwan

Shigetoshi Nakatake

Univ. of Kitakyushu, Japan

Gi-Joon Nam

IBM, USA

Sherief Reda

Brown Univ., USA

Shin'ichi Wakabayashi

Hiroshima City Univ., Japan

Takahiro Watanabe

Waseda Univ., Japan

Evangeline F. Y. Young

The Chinese Univ. of Hong Kong,
Hong Kong

**[7] Timing, Power,
Signal/Power Integrity Analysis
and Optimization**

***Youngsoo Shin**

KAIST, Korea

Emrah Acar

IBM, USA

Shabbir Batterywala

Synopsys, India

Hongliang Chang

Cadence, USA

Masanori Hashimoto

Osaka Univ., Japan

Volkan Kursun

Univ. of Wisconsin, Madison,
USA

Jing-Jia Liou

Nat'l Tsing Hua Univ., Taiwan

Toshiyuki Shibuya

Fujitsu Lab., Japan

**[8] Interconnect, Device and
Circuit Modeling and
Simulation**

***Hideki Asai**

Shizuoka Univ., Japan

Charlie Chung-Ping Chen

Nat'l Taiwan Univ., Taiwan

Yungseon Eo

Hanyang Univ., Korea

Parthasarathy Ramaswamy

Intel, India

Takashi Sato

Tokyo Inst. of Tech., Japan

Sheldon Tan

Univ. of California, Riverside,
USA

Wenjian Yu

Tsinghua Univ., China

**[9] Test and Design for
Testability**

***Seiji Kajihara**

Kyushu Inst. of Tech., Japan

Wu-Tung Cheng

Mentor Graphics, USA

Sungho Kang

Yonsei Univ., Korea

Huawei Li

Chinese Academy of Sciences,
China

Yukiya Miura

Tokyo Metropolitan Univ., Japan

Satoshi Ohtake

NAIST, Japan

**[10] Analog, RF and Mixed
Signal Design and CAD**

***Jaijeet Roychowdhury**

Univ. of Minnesota, USA

Seonghwan Cho

KAIST, Korea

Alper Demir

Koc Univ., Turkey

Kimihiro Ogawa

Sony, Japan

Zhiping Yu

Tsinghua Univ., China

**[11] Leading Edge Design
Methodologies**

***Ing-Jer Huang**

Nat'l Sun-Yat-Sen Univ., Taiwan

Xu Cheng

Peking Univ., China

Koji Inoue

Kyushu Univ., Japan

Shorin Kyo

NEC, Japan

Takashi Miyamori

Toshiba, Japan

Takao Onoye

Osaka Univ., Japan

In-Cheol Park

KAIST, Korea

Li Shang

Queen's Univ., Canada