ASP-DAC 2008 Best Papers

Best Paper Award

1A-1 **Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning**
Feng Wang, Xiaoxia Wu, Yuan Xie (*Pennsylvania State Univ., United States*)

9A-1 **An Efficient, Fully Nonlinear, Variability-Aware Non-Monte-Carlo Yield Estimation Procedure with Applications to SRAM Cells and Ring Oscillators**
Chenjie Gu, Jaijeet Roychowdhury (*Univ. of Minnesota, United States*)

Best Paper Candidates

1A-1 **Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning**
Feng Wang, Xiaoxia Wu, Yuan Xie (*Pennsylvania State Univ., United States*)

2C-1 **Symmetry-Aware Placement with Transitive Closure Graphs for Analog Layout Design**
Lihong Zhang (*Memorial Univ. of Newfoundland, Canada*), Richard Shi (*Univ. of Washington, United States*), Yingtao Jiang (*Univ. of Nevada, United States*)

3A-5 **MeshWorks: An Efficient Framework for Planning, Synthesis and Optimization of Clock Mesh Networks**
Anand Rajaram, David Z. Pan (*Univ. of Texas, Austin, United States*)

5B-1 **Hybrid Solid-State Disks: Combining Heterogeneous NAND Flash in Large SSDs**
Li-Pin Chang (*Nat'l Chiao Tung Univ., Taiwan*)

6A-1 **Pessimism Reduction in Coupling Aware Static Timing Analysis Using Timing and Logic Filtering**
Debasish Das (*Northwestern Univ., United States*), Kip Killpack, Chandramouli Kashyap, Abhijit Jas (*Intel, United States*), Hai Zhou (*Northwestern Univ., United States*)

6B-2 **Within-die Process Variations: How Accurately Can They Be Statistically Modeled?**
Brendan Hargreaves, Henrik Hult, Sherief Reda (*Brown Univ., United States*)

8A-1 **Circuit Lines for Guiding the Generation of Random Test Sequences for Synchronous Sequential Circuits**
Irith Pomeranz (*Purdue Univ., United States*), Sudhakar M. Reddy (*Univ. of Iowa, United States*)

8B-1 **ReSP: A Non-Intrusive Transaction-Level Reflective MPSoC Simulation Platform for Design Space Exploration**
Giovanni Beltrame (*European Space Agency, The Netherlands*), Cristiana Bolchini, Luca Fossati, Antonio Miele, Donatella Sciuto (*Politecnico di Milano, Italy*)

9A-1 **An Efficient, Fully Nonlinear, Variability-Aware Non-Monte-Carlo Yield Estimation Procedure with Applications to SRAM Cells and Ring Oscillators**
Chenjie Gu, Jaijeet Roychowdhury (*Univ. of Minnesota, United States*)

9B-1 **SPKM : A Novel Graph Drawing based Algorithm for Application Mapping onto Coarse-Grained Reconfigurable Architectures**
Jonghee W. Yoon (*Seoul Nat'l Univ., Korea*), Aviral Shrivastava (*Arizona State Univ., United States*), Sanghyun Park, Minwook Ahn, Reiley Jeyapaul (*Arizona State Univ., United States*), Yunheung Paek (*Seoul Nat'l Univ., Korea*)

ASP-DAC 2008 Design Contest Award

Best Design Award

1D-1 A 1.2GHz Delayed Clock Generator for High-speed Microprocessors

Inhwa Jung, Moo-Young Kim, and Chulwoo Kim (*Korea Univ., Republic of Korea*)

Special Feature Award

1D-7 Dynamic Supply Noise Measurement Circuit Composed of Standard Cells Suitable for In-Site SoC Power Integrity Verification

Yasuhiro Ogasahara, Masanori Hashimoto, and Takao Onoye (*Osaka Univ., Japan*)