Designers' Forum

Designers' Forum was conceived as a unique program that shares design experience and solutions of real product designs of the industries among SoC designers and EDA academia/developers.

It consists of these four special sessions.
Oral Sessions:
- 4D New Emerging Application Areas for Future SoC
- 8D Low Power Chips

Panel Discussions:
- 5D Are System Level EDA Tools/Methodologies Coming?
- 9D Best Ways to Use Billions of Devices on a Chip

Here, designs will be presented focusing on design styles, design issues, new technologies, and ways to tackle design issues. Panel discussions will also be held for the latest design issues and EDA methodologies. Detailed information of each session is as follows.

Session 4D (10:15-12:20, January 23) [**New Emerging Application Areas for Future SoC]**
▷ This session deals with new emerging industries. Four speakers will present on future home, automotive, mobile, and environmental electronics. Presenters are from Samsung (future DTVs), NEC (in-vehicle vision processors), Picochip (multi-core DSP for base stations), and Hitachi (wireless sensor networks).

Session 5D (13:30-15:35, January 23) **[Are System Level EDA Tools/Methodologies Coming?]**
▷After more than 10 years of studies by many researchers, system level EDA is still not popular. However, some success stories are reported recently. Issues on modeling/ synthesis/verification and platform-based designs can be discussed in this panel.

Session 8D (13:30-15:35, January 24) **[Low Power Chips]**
▷ In this session, low power chips designed recently will be presented. Static and dynamic power reduction techniques will also be discussed. The speakers are from Hitachi (heterogeneous multi-cores), Synopsys (low power design techniques), NEC (low power application processors for mobile handsets), and Global UniChip.

Session 9D (15:50-17:55, January 24) **[Best Ways to Use Billions of Devices on a Chip]**
▷ Issues on effective use of billons of devices on a chip are the theme of this panel. What to integrate (processors, memories, DSPs, programmable circuits)? How to integrate (buses, networks, protocols, buffers)? Defect tolerant designs and error recovery designs can also be discussed.

Designers' Forum Chair
Hyunchul Shin
(*Hanyang Univ., Korea*)