LVDS-type On-Chip Transmision Line Interconnect with Passive Equalizers in 90 nm CMOS Process

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***Abstract*— This paper demonstrates a low voltage differential signaling (LVDS)-type on-chip transmission line (TL) interconnect to solve delay issues on global interconnects. The proposed on-chip TL interconnect can achieve 10.5 Gbps signaling and has smaller delay, smaller delay variation and better power efficiency than conventional on-chip interconnects at high-frequencies.**

I. Introduction

Interconnect delay has been increasing due to miniaturization of Si CMOS process and constitutes a large percentage of total delay. Interconnect delay and its variation complicate the timing design and limiting the performance of LSI.

Transmission line (TL) interconnects have been proposed to reduce global interconnect delay [1]–[6]. On-chip TL interconnects can perform near-speed-of-light signaling and have much smaller delay than conventional on-chip lines (so-called RC lines). We have developed current mode logic (CML)-type on-chip TL interconnects for applying critical paths [3]–[6]. CML buffers can operate in high frequency and have tolerance to the common mode noise. However, CML buffers have large static power dissipation. The design challenge for the TL interconnect is improvement of power efficiency, which is one of the most important metrics for interconnects from the view point of circuit design.

This paper proposes a low voltage differential signaling (LVDS)-type on-chip TL interconnect with passive equalizers as an RC-line alternative. We will demonstrate the effectiveness and impact of the LVDS-type TL interconnect by comparing to the conventional on-chip interconnects.

II. Interconnect design

Delay and power consumption are important considerations for on-chip TL interconnects. Ideas for improving these portions are discussed as follows.

Figure 1 shows the proposed LVDS-type on-chip TL interconnect. The number of circuit stages in transmitter (TX) and receiver (RX) has to be minimized to achieve small delay and small delay variation. Delay at TL is very small because signals can propagate in electromagnetic-wave speed. Offset delay (delay at line-length of zero) is dominant for TL interconnects, and the reduction of offset delay is the important issue [6].

Figure 2 shows current flows in CML- and LVDS-type TX circuits. Large *Ri*-product is required to achieve large voltage drop, *i.e.* signal amplitude at outputs in the CML-type TX. *R* is determined by impedance matching condition and is almost 50 Ω. The CML-type TX requires large extra current *i* to achieve large *Ri*-product. In the LVDS-type TX, off resistance of transistor is much higher than 50 Ω, and most of currents flow into the TL. Thus, the LVDS-type TX can easily achieve static power consumption rather than the CML-type TX.

The design difficulty of on-chip TL interconnects is large resistance of TL and its frequency dependence due to skin effect. For example, the 5-mm-long TL has attenuation of approximately 8 dB at 10 GHz [9]. Output amplitude of TX is proportional to power consumption, so large signal attenuation and frequency dependence require large power consumption of TX. Loss compensation techniques have been used in off-chip serial-links because frequency dependence of on-board TL has been becoming significant due to increase of signal frequencies. Equalizers can compensate frequency dependence of loss in TL and improve eye-diagram. Thus, the equalization technique contributes power saving of TL interconnect.

The proposed TL interconnect has passive equalizers that consist of small-size inductors and capacitors as shown in Fig. 1. The passive equalizers behave as a high-pass filter. The inductor can have a DC resistance of 50 Ω. DC resistance can be used as terminator at lower frequency, and small-size and low-Q inductor can be used. The capacitor in equalizer reduces common-mode impedance and can improve common-mode noise robustness.

III. Measurement

Figure 3 shows the chip micrograph of a prototype fabricated by using 90 nm Si CMOS process. Figure 4 shows time-domain measurement. The proposed interconnect can achieve 10.5 Gbps signaling as a timing margin is assumed to be 0.2.

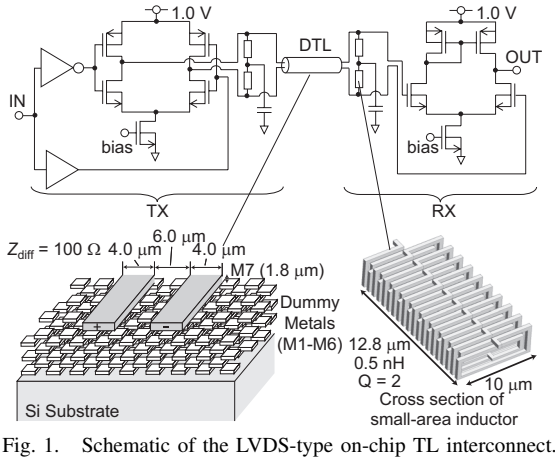
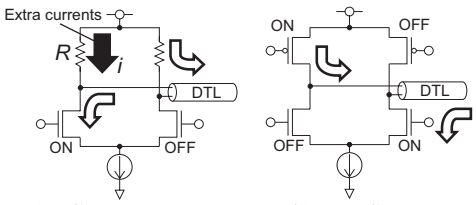


Fig. 1. Schematic of the LVDS-type on-chip TL interconnect.



(a) CML type. (b) LVDS type.

Fig. 2. Current flows in TXs of LVDS and CML interconnects.

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Table I shows performance summary. Measured delay and total power consumption of 5-mm-long TL interconnect are 173 ps and 2.7 mW, respectively.

Figure 5 shows simulated and measured delay and power consumption. Line width and pitch between lines at RC line are minimum sized for the process. Transistor sizes for RC line are designed to minimize delay, and repeaters are inserted every 0.4 mm. Power consumption of TL interconnect is almost determined by static power consumption of TX and RX which does not depend on signal frequency and line length. TL interconnect has smaller delay and power than the RC line at over 2 mm.

Figure 6 shows delay variations. The TL interconnect has much smaller delay variation than the RC line. The TL interconnect does not require repeaters, which can eliminate the delay, delay variation and power consumption of repeaters.

Figure 7 shows a performance comparison. The LVDS-type TL interconnect has the better delay and power efficiency than the other on-chip interconnects.

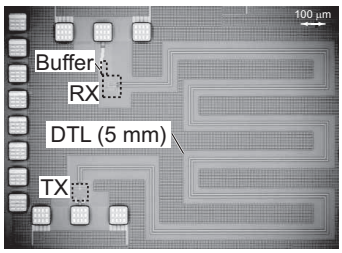
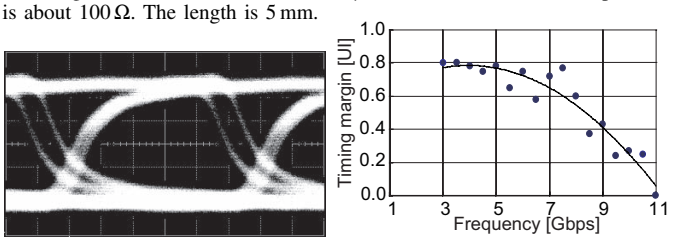


Fig. 3. Micrograph of the test circuit. Total area of TX and RX is 11,100 μm^2 including inductors. Width of DTL is 4 μm. Lossless differential impedance is about 100 Ω. The length is 5 mm.



(a) Eye-pattern at 10.5 Gbps. (b) Timing margin.

Fig. 4. Time-domain measurement. The timing margin is eye-width at bit error rate of 10^{-16} divided by period.

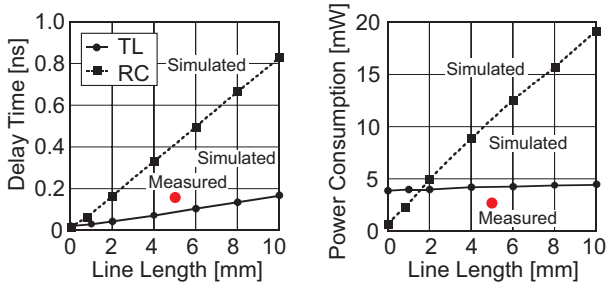


Fig. 5. Delay and power consumption of TL interconnect and RC interconnect. Signal frequency is 10 Gbps.

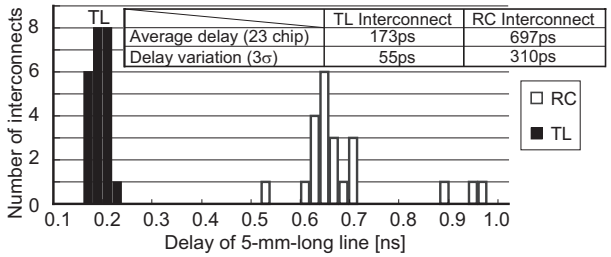


Fig. 6. Measured delay variations of TL interconnect and RC line.

TABLE I

PERFORMANCE SUMMARY.

Process	90 nm Standard Si CMOS
Signal frequency	10.5 Gbps
Average delay of 23 chips	173 ps/5 mm
Power consumption (V_{DD} = 1 V, @10 Gbps)	Tx: 1.9 mW, Rx: 0.8mW Total: 2.7 mW
Energy per Bit (@10 Gbps)	0.27 pJ/bit
Jitter p-p	31 ps
Delay variation	55 ps
Area of TX and RX	11,100 μm^2

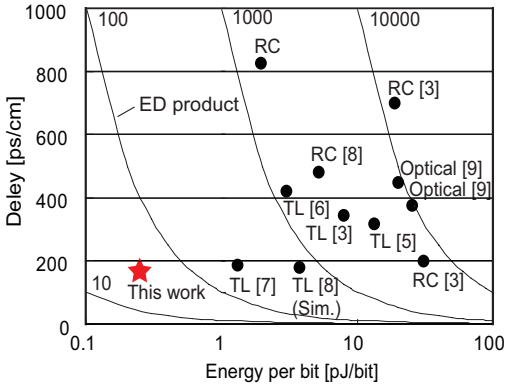


Fig. 7. Performances of on-chip interconnects. Lines of ED products, which are product of delay and energy per bit, are shown. Smaller ED product means better performance [10].

IV. CONCLUSION

The LVDS-type TL interconnect with passive equalizers was proposed to solve delay issues of on-chip interconnects. The proposed TL interconnect fabricated by using 90 nm Si CMOS process can transmit 10.5 Gbps signals. Delay of the TL interconnect is 173 ps/5 mm which is 74 % smaller delay than that of the conventional on-chip line. The TL interconnect has much smaller delay variation than the RC line. The proposed TL interconnect can be one of the most potent candidate for a breakthrough in global interconnect delay issues.

ACKNOWLEDGEMENT

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