A Design- for-Diagnosis Technique for Diagnosing both Scan Chain Faults and Combinational Circuit Faults*

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Abstract - The amount of die area consumed by scan chains and scan control circuit can range from 15%~30%, and scan chain failures account for almost 50% of chip failures. As the conventional diagnosis process usually runs on the faulty free scan chain, scan chain faults may disable the diagnostic process, leaving large failure area to time-consuming failure analysis. In this paper, a design-for-diagnosis (DFD) technique is proposed to diagnose faulty scan chains precisely and efficiently, moreover, with the assistant of the proposed technique, the conventional logic diagnostic process can be carried on with faulty scan chains. The proposed approach is entirely compatible with conventional scan-based design. Previously proposed software-based diagnostic methods for conventional scan designs can still be applied to our design. Experiments on ISCAS'89 benchmark circuits are conducted to demonstrate the efficiency of the proposed DFD technique.

I Introduction

Scan is a widely used DFT technique to improve test and diagnosis quality. The amount of die area consumed by scan chains and scan control signals can range from 15% to 30% [1].

Scan chain diagnosis techniques generally fall into two categories: hardware-based solutions and software-based solutions and tester-based solutions. The software-based solutions can be further classified to Inject-and-Evaluate methods, Signal-Profiling-Based methods. In Inject-and-Evaluate methods [1][5-11], faults are injected into the Circuit-Under-Diagnosis (CUD) to derive the response. Then an algorithm is employed, e.g. the algorithm proposed in [9] or in [10], to score the injected faults by comparing the response from the CUD with the response from the ATE (Automatic Test Equipment). The highest score indicates the most possible fault position. The Signal-Profiling-Based methods [2-4] analyze the signal-1 frequency of each flip-flop to identify the faulty scan cell. Tester-based solutions proposed in [14-15] use tester to control loading and unloading operations and use PFA equipments to observe defective responses to identify a failing scan cell One advantage of software-based solutions is no area overhead. On the other side, shortcomings of software-based solutions include: (1) diagnosis quality depends on the design of the circuit; (2) diagnosis process may be time-consuming especially for the circuit with long scan chains.

In the category of the hardware-based solutions, The work proposed in [20] connects the output of each custom-designed D-type flip-flop (DFF) to the input of its partner DFF. Edirisooriya proposed a work [21], which inserts two-input XOR gates between two scan cells in a scan chain. One input of the XOR gates is driven directly by the output of the preceding cell. The other input of all XOR gates are tied together to be driven by a common signal. Therefore, the state of each scan cell can be flipped by setting/resetting the common signal. Narayanan also proposed a method [22]to set/reset scan cells but by adding a pulse generation circuit into each DFF. Wu proposed a method [23] can diagnose both stuck-at (SA) faults and hold-time faults by connecting a global signal line to every custom-designed DFF so that to simultaneously set and reset these DFFs in an interleaving way. Hardware-based solutions guarantee the diagnosis quality at the price of area overhead or routing overhead.

Unfortunately, none of the above-mentioned solutions can carry on the combinational circuit diagnosis process with faulty chains. Recently, Sinanoglu [13] proposed a diagnosis method to tolerant hold-time faults in scan chains. However, it cannot deal with other fault types. In this paper, a design-for-diagnosis (DFD) scheme named as Helix Scan (HS) is proposed to diagnose scan chain faults and combinational circuit faults. It delivers high diagnosis resolution for scan chain faults. Moreover, the DFD technique enables to apply combinational logic diagnosis techniques to the circuit with faulty scan chains. As we know, the combinational logic diagnosis techniques usually suppose the scan chain is fault free. Using proposed DFD technique, these combinational logic diagnosis techniques can also be utilized

TABLE I
Notations

Upstream	cells index number higher than cell *i*
Downstream	cells index number lower than cell *i*
ChUD	scan chain under diagnosis
Even chain	consists of even indexed scan cells
Odd chain	consists of odd indexed scan cells
EU/OU	upstream cells in even /odd chain
ED/OD	downstream cells in even /odd chain
VFC	virtual faulty chain
VFFC	virtual fault-free chain

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in case of faulty scan chains.

Table Ⅰ lists the notations used throughout this paper.

The rest of the paper is organized as follows. Section 2 introduces the architecture of the proposed Helix Scan. Section 3 presents the procedure of scan chain diagnosis based on Helix Scan. Section 4 further presents the procedure of conducting combinational circuit diagnosis with faulty scan chains. Experimental results are shown in Section 5. Finally, Section 6 concludes the paper.

II. Helix Scan

A. Architecture of Helix Scan

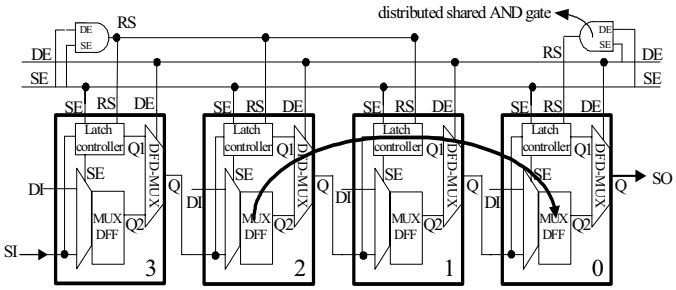


Fig. 1. Architecture of Helix Scan

Fig.1 shows the architecture of Helix Scan. Four HS cells are chained together to form a HS chain. From the scan input to the scan output, each scan cell is given an index number in descending order. For example, the leftmost scan cell in Fig.1 is indexed three labeled at bottom-right, while the rightmost scan cell is indexed zero. We use the same definition of upstream scan cell and downstream scan cell as [1]. For a given scan cell *i*, the cells that are indexed higher than *i* are upstream to cell *i*. The cells that are indexed lower than *i* are downstream to cell *i*. For example, in Fig. 1, given cell *1*, cell *2* and cell *3* are upstream tocell *1* while cell *0* is downstream to cell *1*. The length of the scan chain is the number of scan cells.

Same as the conventional Multiplexed Scan D type Flip-flop (MUX-DFF) scan architecture, *SI* is the Scan-Input signal and *SE* is the Scan Enable signal, both of which are connected to every scan cell. Notice HS has a dedicated diagnosis signal named as Diagnosis Enable (*DE*) which is a global signal. Two distributed shared AND gates are driven by the *DE* and *SE* to produce the *RS* signals. Thus, a HS cell has two additional signal lines compared to the MUX-DFF, which are *DE* and *RS*. The AND gate is shared by neighborhood HS cells which are distributed in a physical region of a given radius *r* surrounding the AND gate. The number of HS cells that share an AND gate is decided by two factors: the layout information after Place & Route and the maximal distance denoted as *r* between AND gate and HS cells. An algorithm can be employed to place AND gates and connect them to their neighbor HS cells under the constraint of minimizing the number of AND gates and routing overhead.

The HS cell has two parts in logical view: the conventional MUX-DFF and the DFD circuitry. The DFD circuitry also has two parts: the latch controller and the DFD-MUX shown in Fig. 1. The input of the latch controller is directly connected with *SI*. The output of the latch controller is Q_1. Under the control of *RS* and *SE*, Q_1 can hold the state of *SI* or the complement state of *SI*. Therefore, the sate related to *SI* can be propagated to its first downstream cell thought DFD-MUX by setting *DE=0*. For example, in Fig.1, the DFD circuitry of cell *1* holds the state of cell *2*' MUX-DFF. It can be propagated to cell *0* by a system clock. As a result, the DFD circuitry can directly propagate the state of MUX-DFF in cell *2* to the MUX-DFF of cell *0*. The data path is illustrated in Fig.1 by bold arrow-head line.

B. Structure of Helix Scan Cell

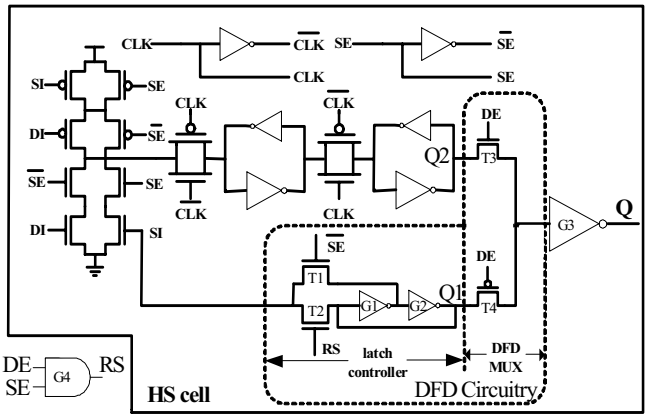


Fig. 2. Hardware organization of Helix -Scan cell

Fig. 2 shows the structure of Helix Scan cell. HS cell consists of two parts: the MUX-DFF and the extra DFD circuitry which is surrounded by dash line. The DFD-MUX comprises *T3* and *T4*. The latch controller comprises *T1*, *T2*, *G1* and *G2*. Assuming each inverter consists of two transistors, we can see that the area overhead of the DFD circuitry is eight transistors.

The truth table of control signals and corresponding outputs are shown in Table Ⅱ. The HS cell has three modes: diagnosis mode, function mode and scan mode. For the purpose of bypassing MUX-DFF, the DFD circuitry should be updated before propagation. Therefore, the HS cell needs to work in scan mode before entering into diagnosis mode. We call the process "+" operation if HS cell propagates *SI* to its first downstream cell, while "-" operation propagates $\overline{SI}$ to its first downstream cell.

TABLE Ⅱ
Truth Table of DFD circuitry in HS Cell

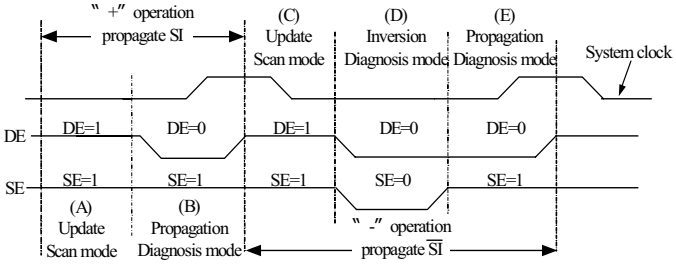
DE	SE	RS	Q1	Q	Mode
0	0	0	$\overline{SI}$	Q1	Diagnosis
0	1	0	Hold	Q1	Diagnosis
1	0	0	$\overline{SI}$	Q2	Function
1	1	1	*SI*	Q2	Scan

C. "+" and "-" operation

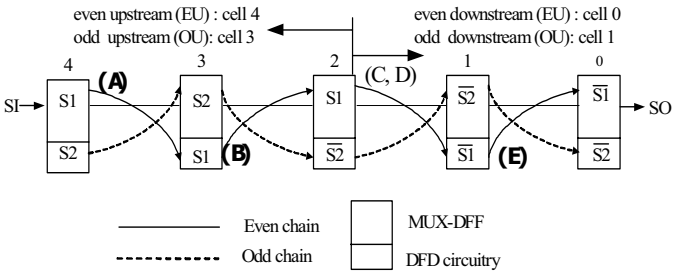
The basic idea of either "+" or "-" operation, is to update the DFD latch and then propagate *SI* or $\overline{SI}$ to its first downstream cell.

The timing diagram of "+" operation followed by "-" operation is illustrated in Fig. 3 (a). "+" operation has two stages called update stage and propagation stage, which is denoted with (*A*) and (*B*), respectively. "-" operation has three stages marked with (*C*), (*D*), and (*E*). Notice (*C*) and (*E*) are similar to (*A*) and (*B*), but (*D*) is an additional stage named inversion stage between update stage and propagation stage. The inversion stage can update the latch in DFD circuitry from *SI* to $\overline{SI}$. (*A*) and (*C*) is the start of "+" and "-" operation respectively, while (*B*) and (*E*) is the end of "+" and "-" operation, respectively. Either "+" or "-" operation starts from scan mode to update the latch controller and ends at diagnosis mode of holding the DFD circuitry. The latch in the DFD circuitry should be held for a while to wait the positive edge of the system clock so that the state of DFD latch can be propagated to the corresponding first downstream cell. To avoid *DI* is held by HS cell in diagnosis or scan mode after the inversion stage of "-" operation, the *SE* signal should be asserted before the positive edge of the system clock.

In Fig. 3 (b), the solid arrow-head line denotes the data path of each stage. (*A*) is marked on the solid arrow-head line between cell *3* and cell *4*, illustrating the update stage of "+"operation during which the cell *3* is updated to *S1* (the state of cell *4*). Then the state of *S1* is propagated to the MUX-DFF of cell *2* during the propagation stage of "+" operation denoted by solid arrow-head line marked with (*B*). Different to "+" operation, the update stage (*C*) and inversion stage (*D*) of "-" operation should be completed when updating the DFD latch of cell *1*, therefore $\overline{SI}$ is propagated to the DFD circuitry of cell *1* instead of *S1*. After propagation stage $\overline{SI}$ is stored in the MUX-DFF of cell 0, which is illustrated by arrow-head line marked with (*E*). Note: as *DE* and *SE* are global signal line, all the scan cells in a scan chain conduct "+" or "-" operation at the same time.



(a) "+" operation (A, B) followed by "-"operation (C, D, E)



(b) Data path of even chain and odd chain. Even chain is denoted the operations in (a)

Fig. 3 Operations and data path of HS cell

It can be see that the state related to *S1* is only propagated to the MUX-DFFs of cell *4*, cell *2* and cell *0* whose index number is even, while the state related to *S2* is only propagated to the MUX-DFFs of cell *3*, and cell *1* whose index number is odd. Therefore, the scan chain can be divided into two logical scan chains. According to the parity of scan cell indexes, even chain and odd chain are defined as follows:

Even chain consists of even indexed scan cells in a scan-chain-under-diagnosis, while odd chain consists of odd indexed scan cells in a ChUD.

Furthermore, for a given scan cell *i*, its upstream cells in even chain are denoted as even upstream (*EU*) cells, and its downstream cells in even chain are denoted as even downstream (*ED*) cells. Similarly, its upstream cells in odd chain are denoted as odd upstream (*OU*) cells, while the downstream cells in odd chain are denoted as odd downstream (*OD*) cells. For the example shown in Fig.3 (b), given cell *2*, then its *EU* cell is cell *4*, *ED* cell is cell *0*, while *OU* cell is cell *3* and *OD* cell is cell *1*. If a fault occurs on even chain, we regard even chain as virtual faulty chain (*VFC*) and odd chain as virtual fault-free chain (*VFFC*), and vice versa.

Ⅲ. Scan Chain Diagnosis

In this section, we introduce the scan chain diagnostic technique based on HS. We use the hypothesis of Single-Stuck-At model (SSA) in a scan chain. However, software-based solutions can be applied to our HS structure to diagnose multiple faults and timing faults. We will discuss them in the future work. With the design of HS cell, the diagnosis procedure is greatly simplified compared to other software-based solutions. The diagnosis procedure has three main steps as shown in Fig. 4.

STEP 1: Load *0011* flush pattern and unload uninterruptedly in Scan mode to screen out the faulty chain. If the response pattern is the same as the flush pattern, then the scan chain is fault-free. Otherwise, a fault may occurs somewhere in the scan chain. As for an SA1 (stuck-at-1) fault, the response pattern is an all-one pattern. While for SA0 (stuck-at-0) fault, the response pattern is an all-zero pattern. That is, after the step 1, we have known the faulty chain and known whether it is an SA0 fault or SA1 fault.

STEP 2: Load an all-zero pattern if the scan chain has an SA1 fault or load an all-one pattern if the scan chain has an SA0 fault, then conduct the "+" operation and unload the response to observe. Assume cell *3* has an SA1 fault. After loading an all-one pattern, the logic values of all downstream cells to cell *3* are distorted to one. Then, "+" operation is conducted. As a result, cell *3* is bypassed and cell *2* is set to *0* as shown in Fig.5. When the pattern is unloaded, cell *2* is zero while other bits are ones. The fault is at the first upstream of cell *2*.

STEP 3: However, if an SA1 fault exists in the scan path between two scan cells or in the DFD circuit, as shown in Fig. 6 (a), when we conduct "+" operation, the state of SA1 is still propagated to the first downstream cell. An all-one pattern is then observed after unloading. So STEP 3 is employed. That is to say, Helix-Scan can distinguish between MUX-DFF fault and DFD circuitry fault.

In this step, load an all-one pattern if the scan chain has a SA1 fault or load an all-zero pattern if the scan chain has a

SA0 fault. Then conduct the "-" operation and unload to observe.

As shown in Fig.6 (b), an SA1 fault is between cell *3* and cell *4*. Then an all-one pattern is loaded. Since SA1 can not distort the logical value *1*, the pattern is loaded correctly. Afterwards, the "-" operation is conducted. All the bits in the scan chain are toggled to zero except cell *3*. When unloading the pattern the upstream cells of cell *3* are distorted to one. As a result, a part-zero-part-one pattern can be observed. The cell corresponding to the boundary position in this pattern is the immediate downstream of the faulty position.

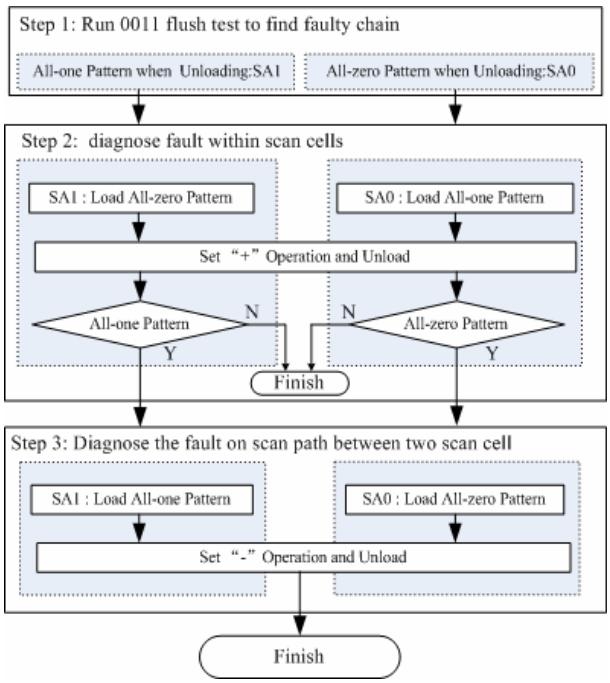


Fig. 4. Scan chain diagnosis flow

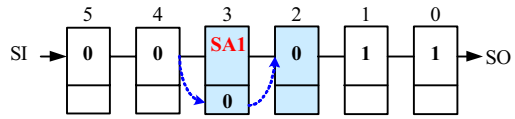
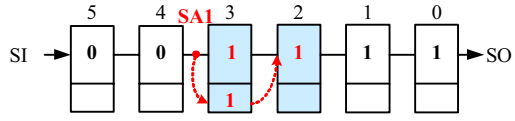
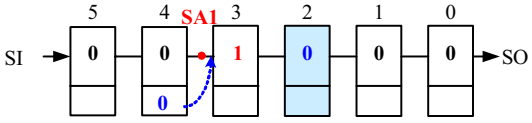


Fig. 5. Diagnose fault in scan cell by "+"operation. SO:*111011*



(a) "+" operation, SO: *111111*



(b) "-" operation, SO: *111000*

Fig. 6 Diagnose fault between two scan cells

IV. Combinational circuit diagnosis with faulty scan chain

With the assistance of HS scan, combinational circuit diagnostic method can be applied to diagnose the circuit with faulty scan chains. "+"or "-" operation is instead of scan shift, therefore diagnostic pattern may need be transformed according to "+"or "-" operations.

As described in Section 2, under the assumption of SSA in a scan chain, a fault occurs either on an odd cell or on an even cell in a faulty scan chain. Therefore, *VFFC* is either an even chain or an odd chain. For example, in Fig.7, cell *4* has an SA1 fault; therefore, odd chain is a *VFFC*, which is denoted by dash-line. The diagnostic pattern of *VFFC* is loaded from *SI*. The *VFC* is an even chain. It is divided into two parts: fault upstream denoted by solid line and fault downstream denoted by dot-dash line. The fault upstream consists of cell *8* and cell *6* whose pattern is loaded from *SI*. The fault downstream consists of cell *2* and cell 0 whose pattern is loaded from DFD circuitry of cell 3 by "+" or "-" operations. That is to say, there are two ports for loading a pattern. One is *SI*; the other is the DFD circuitry. As all the cells conduct "+" or "-" operation at the same time, the patterns loaded from *SI* need to be transformed according to the "+" or "-" operations.

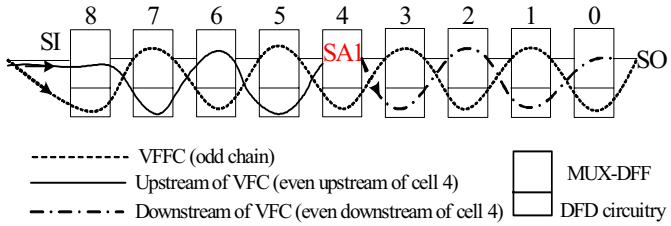


Fig. 7. Pattern loading path of a faulty scan chain

TABLE Ⅲ
Cell state during the loading process

cycle	OP	VFFC					VFC				
							UP			DOWN	
		CeNo.						CeNo.		CeNo.	
		P	7	5	3	1	P	8	6	2	0
0		1	x	x	x	x	x	x	x	x	x
1	+	0	1	x	x	x	x	x	x	x	x
2	+	1	0	1	x	x	1	x	x	x	x
3	-	1	0	1	0	x	1	1	x	0	x
4	-		0	1	0	1		1	0	0	1

For example, if we want to load the scan chain shown in Fig.7 with *100110011*, the state of each HS cells in each cycle are shown in the Table Ⅲ. *OP* in second column represents the operation in each cycle. *UP* and *DOWN* represent fault upstream and downstream of *VFC* respectively. *P* represents the bit is going to be shifted in *VFFC* or fault upstream of *VFC*. As fault downstream of *VFC* is loaded by the DFD circuitry of cell *3*, the *Down* column has no sub-column named *P*. *CeNo* represents cell index number. Each part of faulty scan chain may start loading process at different cycle to guarantee complete loading process at the same time. Therefore, the longest part of scan chain *VFFC* starts to load pattern firstly. In cycle *0*, all the cells are don't-care or

unkonwn (x). The *P* in *VFFC* is one. In cycle *1*, "+" operation is conduct and the data in *P* is propagated to cell *7* and then set *P* to *0*. Similar operation is conducted in cycle *2*. Because both upstream and downstream of fault in *VFC* starts to load pattern in cycle *2*, *P* column in *VFC* is set to *1* in cycle *2*. In the third and fourth cycle, two "-" operations are conducted. The states stored in HS cells are inverted and propagate to its corresponding downstream cells. As for the fault downstream of *VFC*, the first "-" operation sets the DFD latch of cell *3* to *0* and propagate it to cell *2*. The second "-" operation also sets cell *3* to *0* and propagate it to cell *2*. Moreover, the state of the DFD latch of cell *1* is also inverted from *0* to *1* and propagated to cell 0. As a result, pattern *100110011* is loaded into the faulty scan chain. Under the operation of "+", "+", "-" and "-", the pattern shifted in *VFFC* is *1011* and the pattern shifted in fault upstream of *VFC* is *00*.

To be brief, the pattern for fault downstream of *VFC* is loaded by "+"or"-" operation. Then, the patterns for *VFFC* and fault upstream of *VFC* are transformed according to "+"or"-" operations before they are loaded from *SI*.

Ⅴ.Experimental results

A. Performance evaluation of HS cell

We use Hspice to evaluate the latency of HS cell in function mode and scan mode in 0.13um Predictive Technology Model Beta Version technology. In this case, the rising time of HS cell is about 20ps later than that of conventional DFF. The falling time of HS cell is about 60ps latter than that of conventional DFF. However, the clock-to-q time is determined by the rising time, therefore, as a whole, the delay of HS cell is 20ps larger than the delay of a DFF without DFD circuitry.

B. The comparison of area overhead

To evaluate the area overhead of the proposed method, experiments are performed on ISCAS'89 benchmark circuits. Since the layout rules are not available, the measure used for area is the total transistor number. Table Ⅳ lists the area overhead of [20-23] and the DFD method proposed in this paper in addition to the normal scans (MUX-DFF). The best result in Table Ⅳ are in bold face. On average scale, the area overhead of proposed method is 8.95% of the full circuit, which is significantly lower than the area overhead of other methods.

C. The comparison of route overhead

We realized the techniques proposed in [20][21][23] and the proposed HS structure at register-transfer level respectively. Thereafter, Place & Route are conducted by a commercial physical synthesis tool using a standard cell library. Although there is no routing overhead for method proposed in [22], as shown in Table Ⅳ, the area overhead is very large. The additional routing overhead of HS is 11.1%. The overheads of HS are probably over-estimated, because we have to select the worst condition limited by the tools we used: using the HS cell described at register-transfer level instead of costumed HS cell and using extra global signal wire to generate *RS* signal instead of using AND gates. Although the technique in [21] has one global signal line while HS has two in this experiment, HS has smaller area overhead than that of [21], therefore HS also outperforms it in routing overhead on average scale.

D. The diagnosis resolution comparison with software-based solution

To further measure the effectiveness of proposed method, Table Ⅴ shows the average and worst diagnosis resolution of proposed method and software-based diagnosis methods [6] [7] for ISCAS'89 benchmark circuits. The best results are in bold face also. The average diagnosis resolution is the average

TABLE Ⅳ
Comparison area and routing overhead with other hardware-based diagnosis techniques

CUD	Increment of Routing Overhead (%)				Increment of Area Overhead (%)				
	[20] *	[21]	[23]	HS**	[20]	[21]	[22]	[23]	HS
s400	51.8	7.9	17.0	10.2	19.1	22.9	41.9	21	**15.2**
s953	20.7	9.7	10.8	**4.8**	14.2	17.1	31.3	15.7	**11.4**
s1238	19.9	5.8	5.6	**1.9**	6.3	7.6	13.9	6.9	**5.0**
s1488	7.1	1.6	1.3	2.1	1.5	1.8	3.3	1.6	**1.1**
s9234	32.8	12.7	16.5	13.4	8.9	10.7	20.0	10.0	**7.1**
s15850	29.1	17.2	18.2	**16.7**	11.8	14.2	26.0	13.0	**9.5**
s35932	32.0	21.1	24.9	24.0	15.5	18.5	34	17.0	**12.4**
s38584	28.3	15.6	16.6	16.2	12.4	14.9	27.3	13.6	**9.9**
Average	27.7	11.5	13.9	**11.1**	11.2	13.5	24.7	12.4	**8.9**

*in the best condition **in the worst condition

TABLE Ⅴ
Comparison Diagnosis resolution with software-based diagnosis techniques (Average/Worst)

CUD	s5378			s9234			s13207		s15850		s38584	
	HS	[6]	[7]	HS	[6]	[7]	HS	[6]	HS	[6]	HS	[6]
SA0	**1/1.0**	1.0/2	1.6/5	**1/1.0**	1.1/2	1.5/4	1/1.0	1.2/7	**1/1**	1.1/2	1/1.0	1.0/2
SA1	**1/1.0**	1.0/1	1.3/4	**1/1.0**	1.1/2	1.5/4	1/1.0	1.2/5	**1/1**	1.1/2	1/1.0	1.0/2

number of faulty scan cells identified among all scan cells in a circuit. The worst diagnosis resolution is the largest number of faulty scan cells identified among all scan cells in a circuit [7]. The diagnosis resolution of software-based solutions [6] [7] not only depends on the structure of the circuit but also depends on the order of cells and the position of the faulty cell in the scan chain. However, the diagnosis resolution of HS is independent of the circuit. The diagnosis resolution of HS is 1/1.0, which is the best result among these methods.

Ⅵ. Conclusions

This paper proposed a DFD (design-for-diagnosis) technique named Helix Scan (HS), which can not only diagnose faulty scan chains precisely and efficiently but also diagnose the combinational circuit with faulty scan chains. Moreover, the method delivers high diagnostic quality in short time. Our design is entirely compatible with conventional scan-based design and also supports the previous scan chain diagnostic methods. Therefore, multiple faults and timing related faults are also diagnosable. What is more, the conventional diagnostic techniques for combinational circuit which assume that scan chains are faulty free can be applied to the proposed DFD structure with faults in scan chains. Experimental results show the overhead of the DFD techniques is acceptable.

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